GERMANIUM-SILICON ELECTROABSORPTION MODULATORS

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I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

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Abstract

Optical interconnections between electronics systems have attracted significant attention and development for a number of years because optical links have potential advantages for higher speed, lower power, and interference-immunity. With increasing system speed and greater bandwidth requirements, the distance over which optical communication is useful has continually decreased to where the frontier is now at the chip-to-chip and on-chip levels. Successful, monolithic integration of photonics and electronics will significantly reduce the cost of optical components and further combine the functionalities of chips on the same or different boards or systems. At this level, the transmitters and receivers must be integrated directly with Si IC. Modulators are one of the fundamental building blocks for optical interconnects; however, previously no efficient optical modulation mechanism existed in group-IV semiconductors. In order to realize silicon-based group-IV optical transmitters, germanium-silicon electroabsorption modulators are proposed and investigated in this dissertation. Since germanium has a sharp absorption edge with high absorption coefficient due to its unique band structure at the zone center, a Ge quantum well structure is utilized here to provide a strong electroabsorption effect. The epitaxial growth and characterizations of SiGe heterostructures are also studied. SiGe *p-i-n* devices with strained Ge/SiGe multi-quantum-well (MQW) structures in the *i* region are grown on relaxed Ge-rich SiGe buffer layers on silicon substrates. The device fabrication is based on processes for standard silicon electronics and is suitable for mass-production with complementary metal-oxide-semiconductor (CMOS) Si chips. The strongest electroabsorption effect and optical modulation mechanism, the quantum-confined Stark effect (QCSE), is observed in the group-IV semiconductor system for the first time. The absorption edge and coefficients change significantly

with bias voltage. The magnitude of changes is comparable to that of the best III-V materials at similar wavelengths. With proper device structure design, strong electroabsorption is demonstrated over the entire C-band wavelength region, making these devices suitable for telecommunications and also compatible with typical CMOS-chip-operational temperatures. Different modulator configurations are also analyzed and compared. This research will enable efficient transceivers to be monolithically integrated with silicon chips for high-speed optical interconnections.

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Chapter 1 Introduction

1.1 Interconnections

Interconnections provide data transmission channels between nodes at distances ranging from sub-micrometer to thousands of miles (if not counting space communications). Optical interconnections dominate long-distance communications, owing to their advantages for low transmission loss, inherently high carrier frequency, and immunity to interferences. But most short-distance communications still rely on electrical interconnections where electrical signals travel on metal wires or cables. For low data rate communications, the electrical link is a traditional and better solution because of its cost efficiency and manufacturability with silicon chips.

However, the driving force behind the semiconductor industry is the scaling of silicon devices [1], which decreases the size, cost, power consumption of each device and also increases the speed and functionality of integrated chips. It is now difficult for electrical interconnections to achieve equal speed with silicon devices because of their inherent properties as electromagnetic waves with lower carrier frequency similar to their data rate. This imposes a severe challenge to the system performance. In order to match the ever-increasing speed requirements, optical interconnections could provide a better solution [2-7].

We can divide the interconnections into two different levels, depending on not only their distances but also delay models: inter-chip (off-chip) interconnections (RLC model), and intra-chip (on-chip) interconnections (RC model).

1.1.1 Inter-Chip Interconnections

Here inter-chip interconnections include all communications between chips of different systems (such as last-mile, local area networking, storage area networking), different racks or boards, and at the same board as well. In these electrical interconnections, the signals travel inside the transmission lines as transverse electromagnetic (TEM) waves with frequency depending on the data rate. Though the medium is a distributed system, it can be segmented into infinite, serially-connected, lumped RLC models ([See, e.g., ref. [8]). The high frequency makes the propagation delay and loss no longer negligible, even over a short distance, and also the closer proximity causes inter-symbolic interference (ISI) in the same channel. Besides, the mutual inductances existing between transmission lines cause cross-talk between channels.

Electrical interconnections are commonly used for these interconnections because (i) the infrastructure already exists (such as old twisted pair wires for last-mile communications with DSL technology), (ii) it is cheaper and easier to deploy metal wires or cables, (iii) the speed requirement is not stringent and hence the progress of digital signal processing technology makes it feasible to recover the signal from ISI and cross-talk. However, electrical interconnections operating at higher speed require higher power or advanced medium (with lower resistance), which will finally make it economically unfavorable or simply impossible to upgrade systems.

Though 10G Ethernet and storage network are usually thought to be the next penetration point for optical interconnections [9], there is also a tantalizing opportunity for on-board interconnections [10].The bandwidth between a CPU,

memory, and memory controller hub (MCH) chipset shown in Fig. 1.1 already exceeds 6~10 GB/s in today's computer systems (see, e.g., ref. [11]) and keeps increasing. This is even higher than a single 40Gb/s optical channel. If an efficient optical transmitter solution based on CMOS-compatible processes exists, it will be economically viable to be integrated in the core chips (such as chipset or CPU) instead of merely to be used as I/O networking chips, and it will eventually be the solution for all inter-chip interconnections.

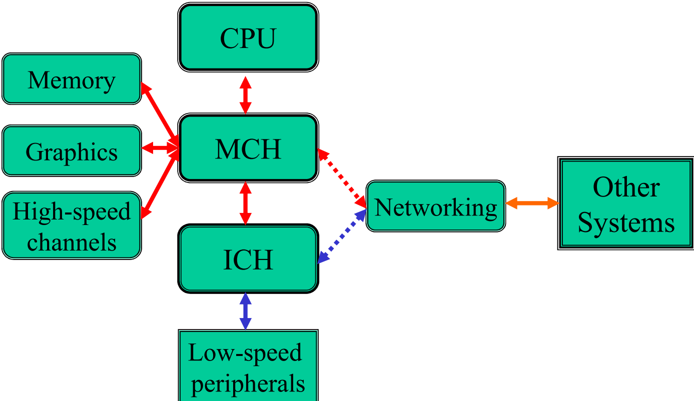

Figure 1.1: A simplified computer system. The networking chip might connect to the memory controller hub (MCH) or I/O controller hub (ICH) chipset, depending on different systems. The links between high-speed chips in the same system might adopt optics after efficient silicon-compatible photonics exists.

1.1.2 Intra-Chip Interconnections

Intra-chip interconnections are used for signaling, clocking, and power-supplying on the same chip. Fig. 1.2 shows the cross-sectional schematic view of a CMOS chip. CMOS devices at the bottom of the chip are connected by local and intermediate wires in the middle levels and by global wires in the top levels. Because metal wires have high resistance and relatively low inductance, the delay of intra-chip interconnections

is RC-limited, where C is the MOS capacitance in the loading stage, and R can be the resistance of metal interconnections, the channel resistance of the MOS device in the driving stage, or the combination of both.

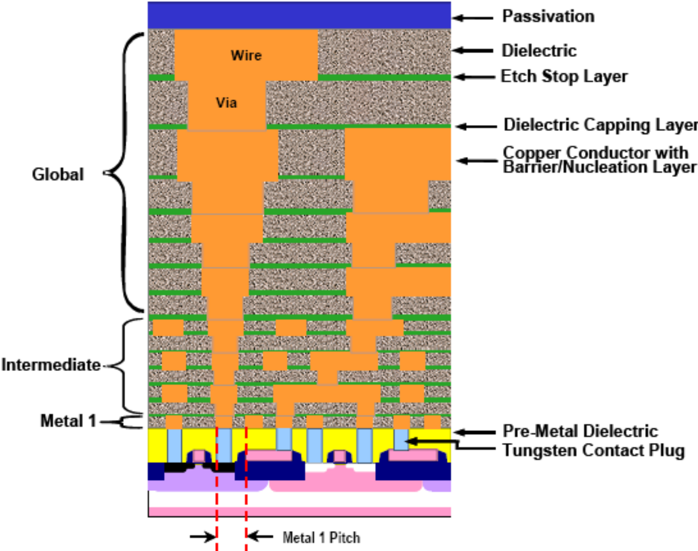

Figure 1.2: Cross-sectional schematic of a CMOS chip. [12]

Fig. 1.3 shows the trends of delay versus technology node predicted by the International Technology Roadmap for Semiconductors (ITRS) [12]. The delays of devices and local interconnections are reduced with the scaling of devices, but the delays of global wires keep increasing [13]. The key reason why global interconnections can not share the same advantages Moore's law brings to all other components is that the cross-sectional area of wires is reduced with each technology node advance, but the length is almost the same, and hence the resistance and delay increase dramatically. In addition, the skin-depth effect at high frequency further limits the conduction cross-section to the outer region of the wires.

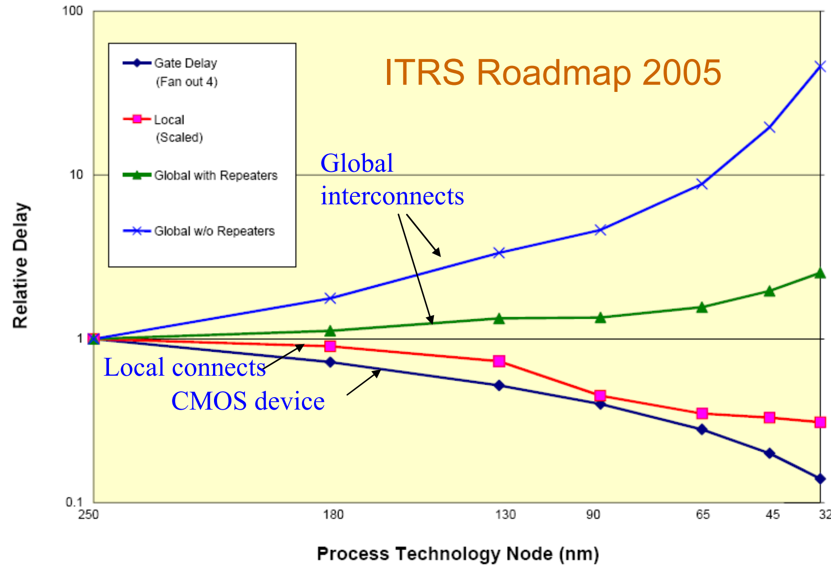

Figure 1.3: Relative delay versus technology node for gate, local interconnects, and global interconnects with and without repeaters. [12]

Even though repeaters [14, 15] are aggressively used to segment the global wire into several shorter sections, the delay cannot be effectively reduced when the technology node reaches the sub 50-nm regime, as shown in Fig. 1.3. This imposes a serious limitation for future CMOS technology to keep using metal global interconnections for signaling and clocking unless much lower cost, integrated optical components are developed.

1.2 Optical Interconnection Systems

In order to realize high-speed inter-chip or intra-chip interconnections, optics would be the best replacement for electrical interconnections if low cost and integration can be achieved. It possesses several advantages: (i) light traveling in a proper medium, such as fibers or free space, has nearly zero power loss over the distance ranges where electrical interconnections still exist (< 1 mile), (ii) light travels at the speed of light

and its delay is minimum, (iii) light is inherently an electromagnetic wave with an ultra-high carrier frequency (as high as 200 THz for a typical 1.5μm wavelength) – it can carry signal without changing its frequency or propagation and it is immune to interferences. This makes light the best carrier for high bandwidth communications.

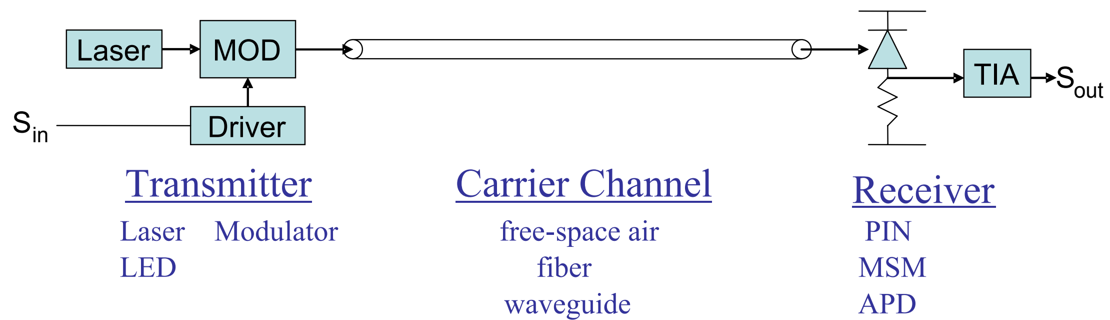

Figure 1.4: Optical interconnection system.

Optical interconnection systems consist of three parts: transmitters, carrier channels, and receivers as shown in Fig. 1.4. The transmitters can be lasers or LEDs alone, or lasers with external modulators. The carrier channels can be silica fibers, free-space air, or waveguides. Existing Si waveguide technology is based on SiGe/Si or silicon-on-insulator (SOI) [16, 17]. The receivers may be p-i-n diodes (low noise, unity responsivity), metal-semiconductor-metal (MSM) diodes (short response time), or avalanche photodiodes (APDs) (high responsivity, but higher noise). Group-IV materials, such as silicon or germanium, have already been used as photodetectors [18]. There is also mature technology for optical carrier channels and receivers based on silicon-compatible technology. The key obstacle to realize optical interconnections is the transmitter. Prior to this work, there was no efficient Si-based modulation mechanism and this function was only implemented by hybrid-bonding expensive III-V compound semiconductor devices. Thus while the optical interconnection systems

were so promising, there was virtually no application of them for short-distance inter-chip or intra-chip communications.

Modulators are favored instead of direct-driven lasers for several reasons. The edge-emitting laser requires a large area, and the vertical cavity surface-emitting laser (VCSEL) requires a sophisticated structure to be fabricated on the top of CMOS chips. Further, in order to modulate the lasers at high bit rates, they must be pre-biased and driven at current densities well above threshold, which consumes high power [19]. The heat generation from lasers is undesired for CMOS chips. The temperature variation in CMOS chips also causes a wavelength shift and this instability can prohibit precise channel allocations for multiple wavelength carriers in the same medium, such as wavelength-division-multiplexing (WDM) schemes. So we prefer to use on-chip modulators as the solution for transmitters and modulate the light coming from an off-chip continuous-wave (CW) laser.

1.3 Optical Modulation Mechanisms

Theoretically light carriers can be modulated in either the amplitude, phase, polarization, or frequency domains. Practically, most modulation is done with amplitude modulation, either by changing the refractive index or absorption coefficient in modulators, because it is difficult for photodetectors to distinguish a change in frequency or phase unless interference techniques are used. The modulation mechanisms can be divided into three categories and their implementations in silicon will be discussed below.

1.3.1 Thermo-Optic Effect

The temperature dependence of the refractive index can be used to implement modulators in a Mach-Zehnder (M-Z) scheme. Two light beams passing through two

separate arms of the M-Z structure have different phase shifts, and then the beams are interfered to produce a combined light wave whose intensity is modulated. This type of thermo-optic switch, usually Si waveguide based on SOI, has been investigated by several groups [20-22]. The temperature of Si is changed by resistive heating to tune the refractive index. There are several drawbacks, including significant power consumption to change the temperature, expensive SOI substrates, and slow transition time (usually ~10 ns).

1.3.2 Electro-Optic Effects

The presence of electric fields or carriers can induce a refractive index change in a material. The mechanisms usually include the Kerr effect and the Pockels effect; the electric-field dependence of refractive index is linear in the former case and quadratic in the later case. There are successful applications based on these, especially in lithium-niobate [23], for optical communications. However, these effects are either weak or completely lacking in group-IV materials. The free carrier plasma dispersion effect [24] using carrier injection was thus used to produce the first over-1GHz silicon modulator on silicon [25]. The structure contains a MOS capacitor on the top of SOI, and light travels in the silicon region confined by the gate and buried oxides. Its operation principle is similar to that of MOS transistors - the gate voltage controls the charge density under the gate oxide, and hence the refractive index can be tuned in the thin charge-accumulated silicon layer. A M-Z structure is used to modulate the light intensity. Owing to the weak effect, the modulator requires a long device length (~several mm) on SOI and a high operation voltage. Another approach based on a ring modulator with the same EO mechanism was demonstrated [26]. The ring structure based on SOI has a smaller size (the diameter, ~12 μm, is three orders of magnitude smaller than the length of the linear waveguide), but requires a very high quality-factor (Q ~ tens of thousands) resonator. This finesse requirement causes two

problems - a very narrow optical bandwidth and severe thermal instability. Since both the linear and ring cavity approaches are based on carrier injection in a forward biased junction, they consume high power.

1.3.3 Electroabsorption Effects

An electric field can also induce changes in the absorption coefficient in a material and hence we can modulate the intensity of light passing through it. The mechanisms include the Franz-Keldysh effect [27, 28] and the quantum-confined Stark effect (QCSE) [29, 30]. The QCSE is especially useful for high-speed [31] or vertical, large-array [32] modulator applications. Unfortunately, no efficient electroabsorption effect had been observed in group-IV materials [33-37] before this work [38]. The detailed principle and previous approaches will be discussed in the next chapter, and then our work will be presented in subsequent chapters.

1.4 Motivation toward Efficient Modulators on Silicon

Optical interconnections can enable high-speed communications; however, we need efficient modulators on silicon to fulfill the key missing part of silicon-based optical interconnections. Previous approaches for thermo-optic or electro-optic modulators on silicon were based on weak physical mechanisms which consume high power, require long optical length or high resonance structures, and are difficult to extend into the projected high-speed regime. Another possibility is the hetero-integration of III-V components with silicon electronics, but the additional fabrication and flip-chip bonding cost make this an economically unfavorable approach compared to monolithic integration. The best solution is a modulator based on an efficient physical mechanism and fabricated in a CMOS compatible process. For this purpose, germanium-silicon electroabsorption modulators are investigated in this dissertation

and show promising results for efficient optical modulators integrated with silicon electronics for optical interconnections.

1.5 Organization

The dissertation reports the study of germanium-silicon electroabsorption modulators aiming for optical interconnections with mass-producible fabrication processes. Chapter 2 discusses the theoretical background for electroabsorption effects as well as SiGe properties and previous SiGe electroabsorption approaches. Chapter 3 presents the Ge/SiGe quantum well structure design which utilizes the unique band structure of Ge for the electroabsorption effect. The effects of structure parameters are simulated by the resonance tunneling method. Chapter 4 discusses SiGe growth, by molecular beam epitaxy and chemical vapor deposition, and material characterization. High-quality Ge quantum wells grown on silicon substrates were demonstrated. Chapter 5 presents the device fabrication processes and reports experimental measurement results. The first strong quantum-confined Stark effect was observed in group-IV material. A heated modulator design is presented to provide C-band operation. Chapter 6 gives a theoretical analysis of different modulator configurations and highlights the efficiency of electroabsorption modulators. Finally, Chapter 7 summarizes this dissertation work and suggests several future directions for further scientific and engineering advances

Chapter 2 Background

2.1 Electroabsorption Effects

2.1.1 Optical Absorption

When light passes through a semiconductor material, its intensity is reduced by absorption processes. The most efficient absorption is based on inter-band transitions, where photons excite electrons to jump from the valence band into the conduction band and generate electron-hole pairs. The processes, shown in Fig. 2.1, can happen in both direct and indirect band gap semiconductors, and the energy and momentum conservation rules must be satisfied.

For the direct band gap transition shown in Fig. 2.1(a), the electrons and holes with minimum energy are at the zone center of k-E band structure. The band edge (minimum energy) absorption generates carriers near $k = 0$ and phonon assistance is not necessary. For the indirect band gap transitions shown in Fig. 2.1(b), the conduction band minimum is not at the zone center, and hence the electron and hole have different k-momenta. The emission or absorption of a phonon must be involved in the absorption process to provide the momentum difference, but this also reduces the transition probability and absorption coefficient.

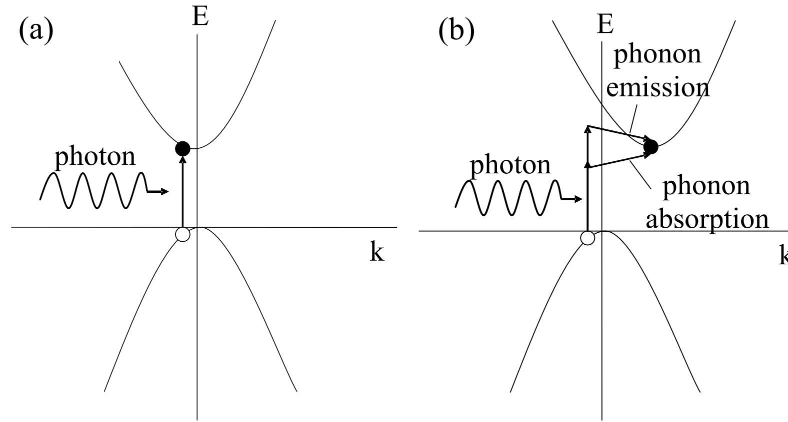

Figure 2.1: (a) Direct band absorption with electrons and holes at the zone center. (b) Indirect band absorption with phonon assistance.

2.1.2 Quantum Well System

A semiconductor quantum well system is constructed by barriers with higher band gap energies and a well with a smaller band gap energy. Carriers, including electrons and holes, are mainly confined inside the well region. For an ideal quantum well grown along the z-axis with infinite barrier heights, the allowable z-direction momentum vectors k_z are quantized and can be expressed as

$$k_z = \frac{n\pi}{L} \quad , \tag{2.1}$$

where L is the width of quantum well and n is the quantum number (a positive integer), and hence the allowable energy states are discrete.

Due to the quantum confinement effect, the energies of quantized states in semiconductors are higher than the bottom of the conduction band for electrons and

lower than the top of the valence band for holes. The separation shown in Fig 2.2 is defined as the "quantum well energy" -

$$E_n = \frac{(\hbar k_z)^2}{2m_z} = \frac{n^2 h^2}{8m_z L^2} \ , \tag{2.2}$$

where m_z is the effective carrier mass along the z-axis and h is the Planck constant.

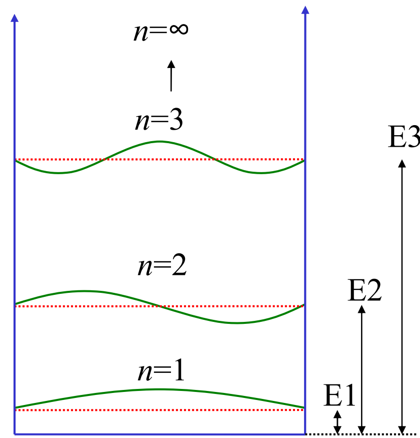

Figure 2.2: Ideal quantum well system with infinite barriers. Carriers' wave functions (green lines) are confined inside well (blue lines) with discrete energy states (red lines).

2.1.3 Excitons

Theoretical band structures are built up without considering attractions between electrons and holes. In a high purity semiconductor, the photon-generated electrons and holes attract each other through the Coulomb force and form excitons. The binding of an electron-hole as an exciton is similar to that of electron-nucleus in a Bohr atom structure. Excitons in bulk semiconductors are called free excitons or Mott-Wannier excitons and are usually only observed clearly at low temperatures (See, e.g.,

[39-40]). The absorption spectrum shows exciton peaks with energies below the normal absorption edge, and the energy difference is the binding energy which can be quantized [40] as a Rydberg equation

$$E^{n}_{3-D,\ ex} = \frac{e^4}{8\varepsilon^2 h^2}\left(\frac{m_e m_h}{m_e + m_h}\right)\frac{1}{n^2} = \frac{E_B}{n^2} \tag{2.3}$$

where e is the elementary charge, m_e and m_h are effective masses of electrons and holes, ε is the permittivity, h is the Planck constant, n is the quantum number (a positive integer), and E_B is the Rydberg binding energy. The exciton binding energies for bulk Si, Ge, and GaAs are 14.7 meV, 4.15 meV, and 4.2 meV respectively [41]. The diameter of excitons are typically in the order of 10 nm; thus an electric field of ~ 10^4 V/cm can ionize them and make their related absorption peaks broaden or disappear.

For a quantum well structure grown along the z-axis, the electrons and holes are confined inside the well regions. The excitons are also squeezed in the z direction and bounded through the Coulomb force in the x-y plane. They tend to become 2-D excitons instead of Bohr-atom-like 3-D excitons. The binding energy in the extreme 2-D case is [40]

$$E^{n}_{2-D,\ ex} = \frac{E_B}{(n-\frac{1}{2})^2}, \tag{2.4}$$

which is larger than that of 3D excitons for the same n-state (though in absorption spectra, the energy of 2-D exciton peaks would be higher than that of 3-D ones due to the quantum well energy). The quantum confinement also increases the spatial overlap of electron-hole pairs and hence the absorption coefficient is larger. The 2-D-like excitons can be observed even at room temperature [42]. The relative absorption

magnitude and edge position between the bulk material, 3-D exciton, and 2-D exciton are compared in Fig. 2.3.

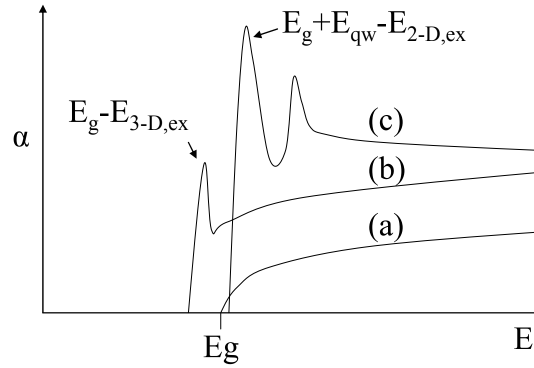

Figure 2.3: Absorption spectra of the same material: (a) without exciton effect (b) with 3-D excitons (c) with 2-D excitons confined in the quantum well. (Not to scale)

2.1.4 Franz-Keldysh Effect

When a strong electric field is applied across a bulk semiconductor, the absorption edge and coefficient can be changed through the Franz-Keldysh effect [27, 28]. There is an absorption tail existing below the band gap energy, and its magnitude and edge shift are increased with the electric field. It is caused by the photon-assisted tunneling of electrons between different spatial locations. For the electron and hole with their locations separated by a distance d along the electric field F, their energy difference is reduced by dF, and hence photons with energy higher than $E_g - dF$ can excite electron-hole pairs into these locations by tunneling. However, the magnitude is relatively small unless the electric field is higher than 10^5 V/cm, thus it is not an efficient modulation mechanism.

2.1.5 Quantum-Confined Stark Effect

The quantum-confined Stark effect (QCSE) [29, 30] is the most efficient optical modulation mechanism. Fig 2.4 illustrates its basic principle.

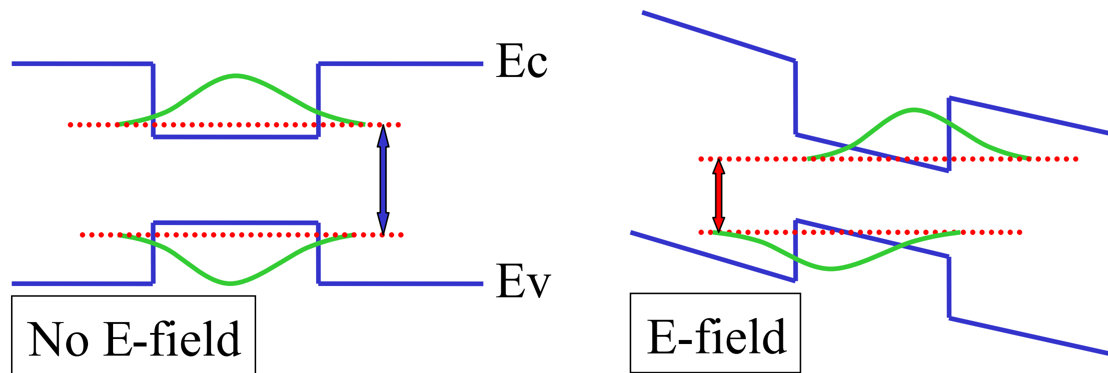

Figure 2.4: Quantum well (blue lines), carriers' wave functions (green lines) and states (red dash lines), and transition energy (arrows) with and without electric field influence.

Without the presence of an electric field, the wave functions of ground-state electrons and holes and their probability densities are concentrated and symmetrically distributed inside the well. This gives strong coupling between electrons and holes as well as high band-edge absorption strength. When an electric field is applied across the quantum well, the band is no longer flat. Electrons and holes are swept to opposite sides of the well, so their coupling is largely reduced. Besides, the quantum well energy also decreases with respect to the center of the well, thus the transition energy is reduced. This results in two main characteristics of the QCSE – the Stark (red) shift of the absorption edge and a reduction of the band edge absorption coefficient.

Electrons and holes (not shown in Fig. 2.4) at higher states would also contribute to the absorption if the selection rule allows their transitions. Under a high electric field, some forbidden transitions (such as even-symmetric electrons to odd-symmetric holes, or odd-symmetric electrons to even-symmetric holes) start to appear.

Though the absorption coefficient near the band edge absorption is lowered under the biased condition, the number of total carriers is still the same, thus the total

absorption probability is not changed. This "unity sum rule" can be observed in the integration of absorption coefficient through the energy domain [43].

The QCSE is more significant when considering a 2-D exciton effect. When an electric field is applied parallel to the quantum well layers, excitons start to be ionized and the resonance width increases; when the field is higher than ~10^4 V/cm, the exciton absorption peaks broaden and finally disappear, just like the behavior of 3-D excitons. However, when an electric field is applied perpendicular to the quantum well layers as illustrated in Fig 2.4, the barrier confine carriers inside the well even under a high electric field, so electrons and holes remain bounded and excitons can still exist unless the electric field is larger than ~10^5 V/cm [29]. The QCSE strength is sensitive to the polarization of light [30, 44]. Theoretically [44], for the transverse electric (TE) mode polarization, the heavy hole (HH) exciton strength is 3 times that of the light hole (LH) transition; for the transverse magnetic (TM) mode polarization, only the LH exciton transition is allowable, the HH transition is forbidden because its momentum element projection at the band edge is zero. But the total matrix-elements of HH and LH are the same due to the sum conservation [43] as in the bulk case.

In an infinite quantum well system, the quantum well energy under an electric field can be approximated by the perturbation method. The energy reduction and Stark shift in the ground state transition can be expressed as [45, 39]

$$\Delta E = \frac{\pi^2 - 1}{24\pi^4}(m_e + m_h)\frac{e^2 F^2 L^4}{\hbar^2} \tag{2.5}$$

where L is the width of quantum well, m_e and m_h are effective masses of electrons and holes, F is the applied electric field, e is the electron charge, and $\hbar$ is the reduced Planck constant. The quadratic dependence in the electric field and the 4th-power dependence in the quantum well width are caused by the second-order perturbation due to the absence of the first-order correction in even-symmetric eigenfunctions.

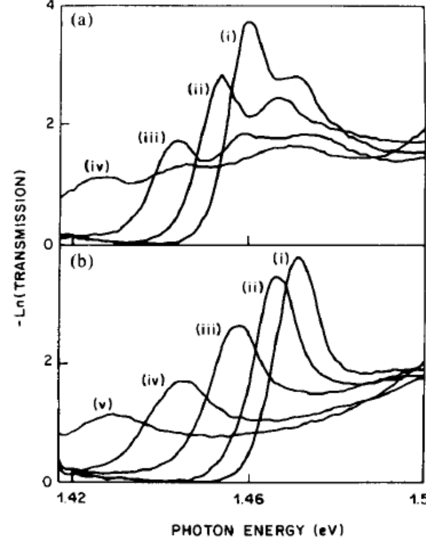

Figure 2.5: Typical QCSE in III-V semiconductors. Absorption spectra of GaAs/$Al_{0.3}Ga_{0.7}As$ QW under an electric field increasing from (i) to (v) with light polarization in (a) TE mode (b) TM mode. [30]

The refractive index (*n*) and absorption coefficient (α) are proportional to the real and imaginary parts of $\sqrt{\varepsilon_r^{'} + j\varepsilon_r^{''}}$ (the square root of the complex form of the dielectric constant), which corresponds to the real part (χ') and imaginary part (χ'') of the complex form of susceptibility. The χ' and χ'' can be correlated through the Kramers-Kronig relations (see, e.g., ref. [39, 40]) as

$$\chi'(\omega) = \frac{2}{\pi} P \oint \frac{y\, \chi''(y)}{y^2 - \omega^2} dy \tag{2.6}$$

$$\chi''(\omega) = -\frac{2\omega}{\pi} P \oint \frac{\chi'(y)}{y^2 - \omega^2} dy\ , \tag{2.7}$$

where P is the principal value of the Cauchy integral, so the change of the band-edge absorption coefficient by the QCSE also causes the change of the refractive index, and vice versa. But the refractive index change is not nearly as strong compared to the large change in magnitude in the absorption coefficient.

2.2 SiGe Material System

Previously semiconductor-based optical transmitters, such as lasers or QCSE modulators, were almost all based on III-V compound materials. However, in order to integrate photonics with silicon electronics, it is necessary to realize the QCSE in the silicon-germanium material system. Both Si and Ge are group-IV semiconductor materials, and silicon is the fundamental building material for the information industry. The addition of Ge into Si forms SiGe alloys and their heterostructures improve the electrical properties [46, 47], so both materials are used in today's chip fabrication processes [48].

2.2.1 Band Structures

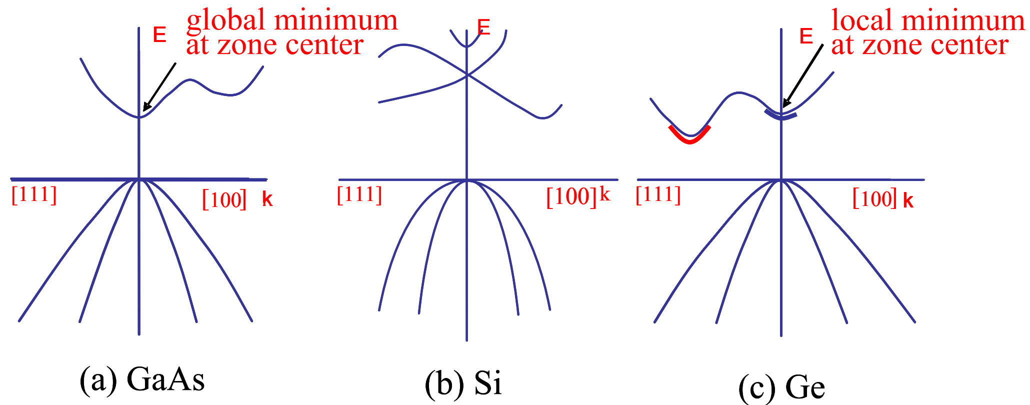

Figure 2.6: Simplified k-E band structures of bulk semiconductors: (a) GaAs (b) Ge (c) Si.

The band structure is the fundamental property which determines the optical efficiency in a semiconductor material. Most III-V compounds, such as GaAs shown in Fig. 2.6(a), are direct band gap materials with both global minima of the conduction and maxima of the valence bands at the zone center of the band structure. They can emit light through the radiative recombination of electrically-injected carriers as well as absorb light through the zone-center transition, so most optical applications, including

light emission, photodetection, and QCSE modulation, are possible and efficient. For silicon, shown in Fig. 2.6(b), the global minimum of its conduction band is not at the zone center [49, 50], thus its optical processes are dominated by the indirect band transition and all optical efficiencies are very poor. For germanium shown in Fig. 2.6(c), it is interesting that though the lowest global minimum of its conduction band is also not at the zone center, there still exists a local minimum at the zone center (like the Kane-shaped structure in direct band semiconductors) with an energy position just above the global minimum [49, 50]. The room-temperature absorption edges related to the direct and indirect transitions are ~ 0.8 eV [51] and ~0.64 eV respectively [52]. Fig. 2.7 shows the bulk absorption coefficient spectra versus the photon energy and wavelength for important semiconductors at room temperature [53]. The absorption coefficient of Ge is ~ 5000 cm^{-1} at ~ 0.8 eV (1550 nm), and its absorption edge is very steep even though a weak indirect band absorption tail exists. The magnitude of the absorption coefficient and the edge sharpness in Ge is comparable to that in GaAs or InAs. This high absorption efficiency of Ge comes from its Kane-shaped band structure at the zone center [54] similar to the direct band gap III-V compounds.

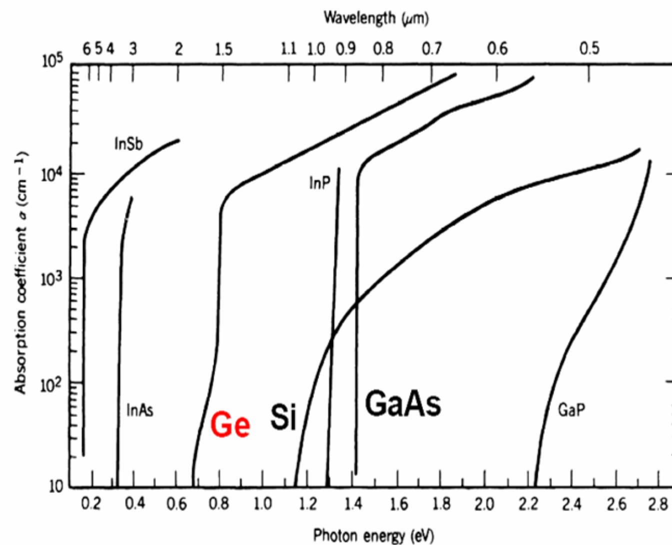

Figure 2.7: Bulk optical absorption coefficient spectra of major semiconductor materials. [53]

2.2.2 SiGe Heterostructures

2.2.2.1 Band Structure of SiGe Alloy

The crystal structure of Si and Ge are diamond-like with band gap energies 1.12 eV and 0.66 eV at room temperature respectively. The conduction band minima are at the Δ points (the [111] direction) for Si and at the L points (the [100] direction) for Ge (See, e.g., ref. [55]). Si and Ge are miscible in all compositions to form SiGe alloys, whose band structures as well as electrical and optical properties become mixed and complicated, owing to the different conduction band origins. Fig 2.8 shows the band energies of relaxed SiGe [56]. Most of the band shift is in the valence band because the electron affinity energies of Si and Ge are 4.05 and 4.00 eV respectively [57]. The conduction band minima transit from the Δ points near the Si-end into the L points near the Ge-end, and the transition point is at around $Si_{0.15}Ge_{0.85}$.

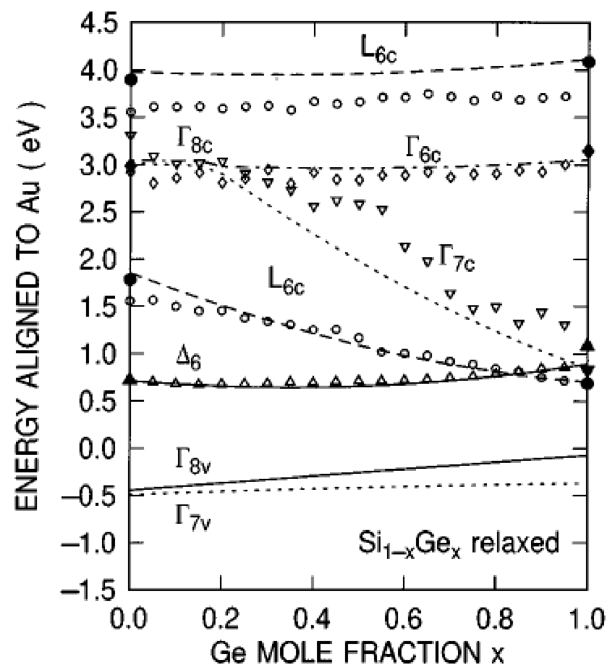

Figure 2.8: Band energies of relaxed SiGe alloys. Lines are simulated results by pseudo-potential band structure calculations, and symbols are experimental results. [56]

2.2.2.2 Band Alignment in SiGe Heterostructures

The lattice constants of Si and Ge are 0.543 and 0.5658 nm respectively. The high lattice constant mismatch makes the SiGe material deposited on either Si or different-composition SiGe layer strained, unless it is relaxed by generating dislocation defects. The strain force can shift the energy bands, change carrier effective masses, and split valence bands and Δ valleys (see, e.g., ref. [47][56][58]).

The biaxial tensile (or compressive) strain on the SiGe layer can be decomposed into a hydrostatic tensile (or compressive) stress and a uniaxial compressive (or tensile) stress along the growth direction. The hydrostatic tensile (or compressive) stress lowers (or lifts) all conduction bands and lifts (or lowers) all valence bands. The uniaxial stress has no effect in the average band energies, but it breaks the degeneracy of the valence bands into the heavy hole and light hole bands as well as splits the 6-fold Δ valleys into 2 Δ_2 (parallel to the growth direction) and 4 Δ_4 valleys (perpendicular to the growth direction). Under the uniaxial compressive stress, the light hole becomes the topmost valence band, and the Δ_2 valley is lower than the Δ_4 valleys; under the uniaxial tensile stress, the opposite happens. The band gap energy associated with the Δ valley might decrease or increase with the biaxial strain due to the complex conduction band structure, but the band gap energy associated with the L or Γ valley (more relevant to our interest in Ge-rich SiGe structures) would increase (or decrease) with the compressive (or tensile) biaxial strain.

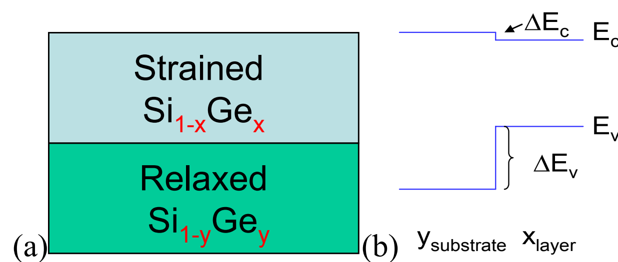

Figure 2.9: (a) heteroepitaxy of strained $Si_{1-x}Ge_x$ layer on relaxed $Si_{1-y}Ge_y$ buffer. (b) Typical band alignment (when x>y).

When a strained $Si_{1-x}Ge_x$ layer is deposited on a relaxed $Si_{1-y}Ge_y$ buffer as shown in Fig 2.9(a), their bands line up as shown in Fig 2.9(b). Most of the band offset is in the valence band, and the valence band maximum is always in the SiGe layer with the higher Ge concentration. The conduction band offset is relatively small, and its minimum might be in the low Ge-concentration region though it usually has a higher band energy. The abnormal conduction band discontinuity and alignment in the SiGe system will be discussed in the next section (Sec. 2.3.3).

2.3 Why No Efficient QCSE in Previous SiGe Systems?

Since the QCSE is the most efficient optical modulation mechanism, researchers had previously tried various approaches to realize this in the SiGe material system. The investigations, prior to this work, could be divided into two categories based on the quantum well alignment – the type-I system, and the type-II system – but all of them were based in Si-rich alloys, hence a relatively inefficient indirect band absorption.

2.3.1 Type-I Aligned Quantum Well

The type-I aligned quantum well system has both the conduction band minimum and the valence band maximum in the same layer. Its QCSE behavior is similar to that discussed in Sec. 2.2. Typical examples in SiGe materials were Si-rich SiGe quantum well structures grown on Si [33-35]. Because their absorption was based on the indirect band transition and the electron confinement was weak (due to the small conduction band discontinuity), their QCSEs were inefficient or absent, even though they were all type-I aligned.

2.3.2 Type-II Aligned Quantum Well

The type-II aligned quantum system has the conduction band minimum and the valence band maximum in different layers. Some researchers used type-II SiGe systems, such as strained SiGe/Si quantum wells on relaxed SiGe buffers [36] or Ge quantum dots on Si substrates [37]. The holes are still confined in the Ge-rich wells, but the electrons stay in Si barriers where the conduction band minimum is lower due to the strain effect (and the confinement is also shallow).

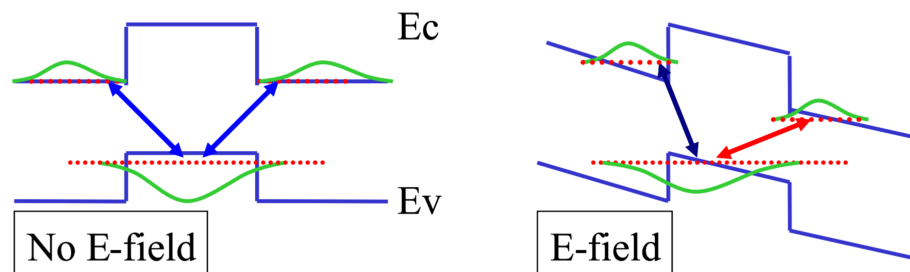

Figure 2.10: QCSE in a type-II aligned quantum well. Both blue and red shifts occur in the transitions under an electric field.

Fig 2.10 shows the transitions in a type-II aligned quantum well with/without an electric field. Since electrons and holes are spatially confined in different layers, abnormal QCSE phenomena would be observed – under an electric field, the transition energy in one side of the quantum well decreases as the typical QCSE behavior, but it increases in the opposite side and a part of the absorption spectrum is blue-shifted. Usually the absorption edge shift is large in the type-II aligned system; however, the absorption coefficient is very small, owing to the weak coupling of spatially separated carriers, thus it is actually not practical for modulators.

2.3.3 Toward Pure Ge Quantum Wells

Fig. 2.11 shows the contours of conduction band offsets (ΔE_C) between the strained $Si_{1-x}Ge_x$ and relaxed $Si_{1-y}Ge_y$ layers (see Fig. 2.9) as well as the compositions of SiGe QCSE approaches. For x > y, a positive (and negative) value of ΔE_C denotes the type-II (and type-I) alignment, and vice versa for x < y. It can be shown that most SiGe heterostructures have type-II alignment, or type-I alignment but shallow confinement, owing to the strain effect and similar vacuum energies in Si and Ge. This explains why previous approaches did not function well because (i) all used the indirect band absorption with low optical efficiency; (ii) Si-rich SiGe heterostructures might be type-I aligned, but their electron confinement was weak and the high-Si content further reduced the absorption coefficient; (iii) the high strain in Ge-rich SiGe caused type-II alignment which further lowered the optical efficiency.

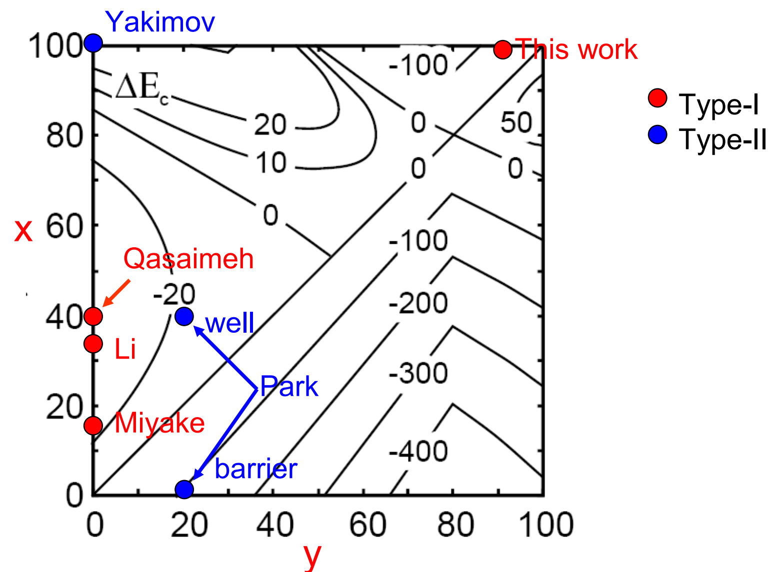

Figure 2.11: Conduction band offsets in SiGe heterostructures and SiGe QCSE approaches. x and y denote the Ge content in the strain epi-layer and relaxed buffer as shown in Fig 2.9. Blue and red dots denote the quantum well and buffer compositions in previous SiGe QCSE approaches and this work (offset contours from ref. [47], data points from [33-38]).

In order to have high Ge content for high absorption efficiency and also to prevent type-II alignment, the upper right corner of Fig. 2.11 becomes the area of choice investigated in this work.

Chapter 3 Germanium Quantum Well Structure

3.1 Design of Type-I Ge Quantum Well Structures

Electroabsorption modulation based on the quantum-confined Stark effect is the strongest optical modulation mechanism and more pronounced for direct band absorption in type-I aligned quantum wells. Both Si and Ge are indirect band gap materials because their global minima in the conduction band are not at the zone center, and hence the indirect band gap absorption between the holes at the zone center and the electrons out of the zone center requires phonon assistance to achieve momentum conservation. This kind of indirect band absorption is inefficient due to the low coupling probability, thus its absorption coefficient near the band edge is low and no clear absorption edge is present. Though Ge is an indirect band gap material, it has a local minimum in the conduction band at the zone center. This allows Ge to have efficient direct band gap transitions with high absorption efficiency as shown in Sec.2.2.1 [53]. Equally important is that this direct conduction band minimum is not much higher than that of the global indirect band minimum, so the absorption

coefficient ratio between the direct band and the indirect band at the direct band edge (~0.8eV) is still high enough such that a sharp absorption edge can be observed in Ge. This Kane-shape band structure of Ge at the zone center is similar to that of direct band gap III-V compound materials, such as GaAs or InAs, and hence we utilized this feature to band-gap engineer the Ge quantum wells for the quantum-confined Stark effect.

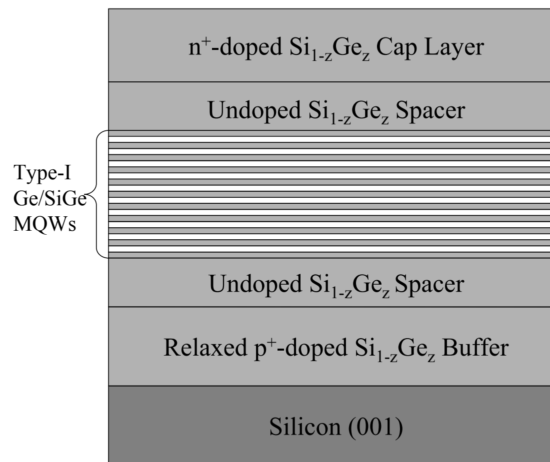

Figure 3.1: A SiGe p-i-n structure on silicon with $Ge/Si_{1-x}Ge_x$ quantum wells on relaxed $Si_{1-z}Ge_z$ buffer.

Due to the 4% lattice mismatch between Si and Ge, Ge layers directly grown on silicon tend to become partially-relaxed layers or quantum dots to relieve this strain energy – the strain and confinement are difficult to control in both cases and are undesired for electroabsorption applications. Even if the Ge layer remains un-relaxed, the high strain force can lift its conduction band and result in type-II alignment. In order to solve this problem and to have type-I aligned quantum wells (see Sec. 2.3.3), a relaxed Ge-rich SiGe layer was used here as the intermediate buffer between the Ge quantum wells and Si substrate.

Fig. 3.1 shows the basic device structure for electroabsorption modulations. The p-i-n device allows the applied voltage to induce uniform electric field across the

Ge/SiGe quantum wells embedded inside the intrinsic region and to change the band-edge absorption characteristics for optical modulation. In addition, a structure of strain-balanced Ge/$Si_{1-x}Ge_x$ multiple-quantum-wells (MQWs) on a relaxed Ge-rich $Si_{1-z}Ge_z$ buffer was used (further discussed in Sec. 4.7). The weighted average of silicon concentration in the Ge/SiGe MQW region is equal or close to that of the buffer layer (which means $x > z$), thus producing compressive strain in the wells and tensile strain in the barriers which are balanced.

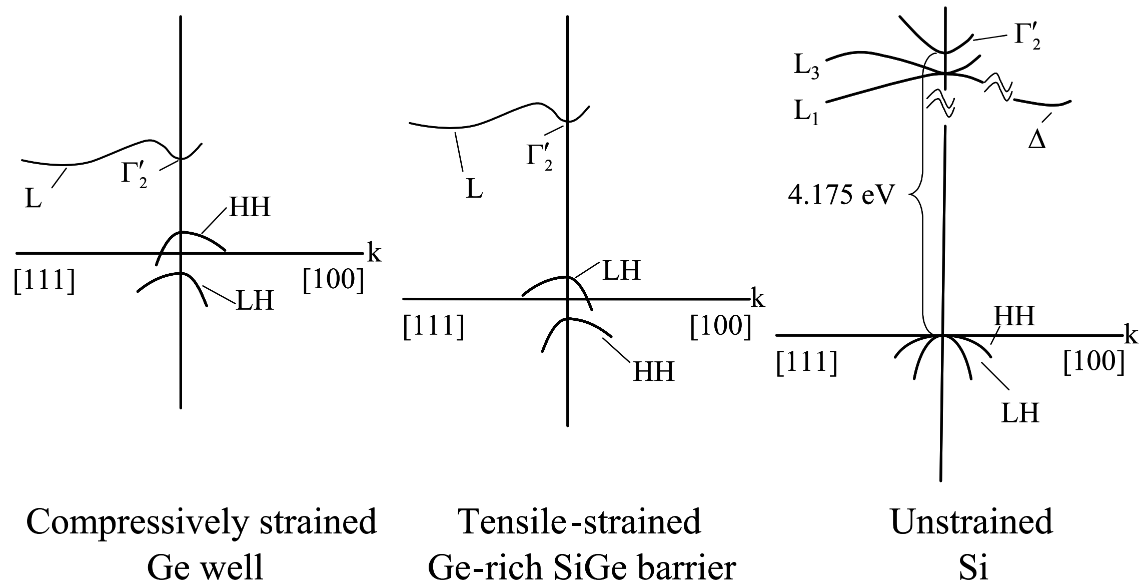

Figure 3.2: Sketch of the band structure (not to scale) of the well (compressively in-plane strained Ge) and barrier (tensile in-plane strained Ge-rich SiGe) materials, and of unstrained Si. HH (LH) – Heavy (Light) Hole band.

The k-E diagrams of Fig. 3.2 illustrate the band structures of the material layers relevant to Fig. 3.1, including the Ge well, SiGe barrier, and Si substrate. The Γ'_2 point shown in all sketches is the conduction band minimum of Ge at the zone center [59]. The silicon substrate is unstrained, thus its heavy hole and light hole bands are

degenerate. Its global conduction band minima are at the Δ points, out of the zone center and far below the direct conduction band minimum. The conduction band structures of the strained Ge well and Ge-rich SiGe barrier are still like that of bulk germanium (see Sec. 2.2.1). Their global conduction band minima are L valleys because of high Ge concentrations. Though the conduction band edge of Ge at the zone center is higher than that for the L valleys, the Kane-shape structure gives it strong absorption. The strain breaks the degeneracy of their valence bands – the compressive in-plane strain in the wells lifts the heavy hole and lowers the light hole; the tensile in-plane strain in the barriers has the opposite effect. In addition, the higher silicon content in the SiGe barriers also increases their band gap energy, mainly in the valence band. Fig. 3.2 also shows this trend - the zero energy point of the valence band (the origin point of the k-E diagram) in each layer is lowered when the Si concentration is increased.

3.2 Band Structure of Strained Ge/SiGe MQWs on Relaxed SiGe Layer

3.2.1 Band Line-Up

Fig. 3.3 shows the band structure of a type-I aligned, strained Ge/SiGe quantum well on a relaxed Ge-rich SiGe buffer layer (the structure of Fig. 3.1). Since the Ge well (and SiGe barrier) is compressively (and tensile) strained, its valence bands are split and leave the heavy hole (and light hole) on the top of the valence bands. There is no strain on the relaxed SiGe buffer, so its valence bands remain degenerate. For the conduction band part, here the global minima of the buffer and barriers are at the L valleys (with a higher Si-content they might become the Δ valleys - the transition point is $Si_{0.15}Ge_{0.85}$ without strain) and lower than that at the zone center (the Γ point). This design owns several advantages. The pure Ge quantum well with the highest Ge

concentration has the highest absorption efficiency and sharpest edge. The compressive strain makes the heavy hole the topmost valence band in the Ge well, which has a stronger Stark shift due to its heavier effective mass (see Eq. (2.5)). The Ge-rich buffer layer prevents the Ge/SiGe quantum well with such high Ge concentrations from suffering such high strain as to cause type-II alignment, so the normal type-I line-up can be achieved for both direct and indirect bands in this quantum well design. Moreover, the Γ point of the Ge well is even higher than the L valleys of the SiGe barriers. This design has dual conduction band confinements: strong confinement for electrons associated with the direct band gap optical processes, and weak confinement for electrons in the indirect band associated with the carrier transport. This helps photo-generated carriers being scattered into the L valley and being swept out by the electric field more easily.

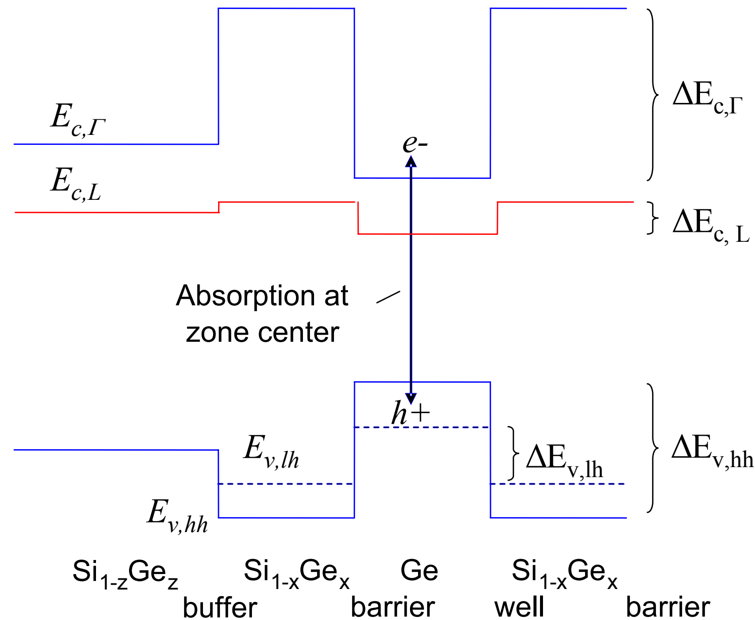

Figure 3.3: Sketch of the band structure in real space (not to scale) of a Ge/SiGe quantum well structure, with compressive strain in the well and tensile strain in the barrier, on a lattice-relaxed SiGe buffer. $E_{v,lh}$ and $E_{v,hh}$ are the valence band edges of the light hole and the heavy hole respectively. $E_{c,\Gamma}$ and $E_{c,L}$ are the conduction band minima at the zone center (the Γ point) and at the L valleys. ΔE represents their band discontinuity.

3.2.2 Band Parameters

The band parameters, including the band gap structure, alignment, and effective masses, in each layer of the structure shown in Fig. 3.3 are important for both intuitive designs and theoretical simulations.

Valence Bands: The valence band offsets for a strained $Si_{1-x}Ge_x$ layer on a relaxed $Si_{1-z}Ge_z$ layer can be expressed as [60]

$$\Delta E_{hh}\left(x,z\right)=\left[0.74-0.07z\right]\left[x-z\right] \tag{3.1}$$

$$\Delta E_{lh}\left(x,z\right)=-0.3z+0.289z^2-0.142z^3+\left(0.683-2.58z+3.21z^2-1.24z^3\right)x$$
$$+\left(0.435+0.704z-2.439z^2+1.295z^3\right)x^2+\frac{\left(-0.354-3.77z+8.79z^2-2.46z^3\right)}{\left(1-2.7z+28.1z^2\right)}x^3 \tag{3.2}$$

if $z > 0.5$ and $\left|x-z\right|\leq 0.5$, which covers the SiGe composition range of our interests.

Since the $Si_{1-z}Ge_z$ buffer is relaxed, the valence band maxima of its heavy hole and light hole remain degenerate. The valence band energy positions of the strained Ge well and SiGe barrier to the relaxed $Si_{1-z}Ge_z$ buffer can be calculated using Eq. (3.1) for the heavy hole and Eq. (3.2) for the light hole, thus the offsets of the heavy hole and light hole valence bands, $\Delta E_{v,hh}$ and $\Delta E_{v,lh}$, between the well and barrier can be extracted.

Direct Conduction Bands: The direct band gap energies (with the relevant conduction minimum at the Γ'_2 point) of bulk Ge and Si are 0.8 eV and 4.175 eV respectively at room temperature. The direct band gap energy of SiGe is linearly interpolated between the value of bulk Ge and Si here, thus the band offset between the Ge well and $Si_{1-x}Ge_x$ barrier can be expressed as

$$\Delta E_{c,\Gamma}=(4.175-0.8)x-\Delta E_{v,hh}\,. \tag{3.3}$$

Though this is based on an interpolation and does not consider the strain effect on the conduction band, the simulation in the next section will show that the uncertainty here would only cause negligible changes in the quantum well energy and shift, owing to the high conduction band offset.

Indirect Conduction Bands: The indirect band gap and alignment is not critical to the optical absorption here. However, the band structure of the relaxed SiGe buffer can be found in Sec. 2.2 (especially Fig. 2.8 which shows the band gap energy), and the indirect conduction band offset between the strained Ge well (or the SiGe barrier) and the relaxed buffer is shown in Fig. 2.11 [47, 58, 60].

Effective Masses*:* The effective masses of $Si_{1-x}Ge_x$ are linearly interpolated between the values of Si and Ge. Their values along the growth direction at the Γ point are $0.041m_o+0.115(1-x)m_o$ [49], $0.28m_o+0.21(1-x)m_o$ [55], and $0.044+0.116(1-x)m_o$ [55] for the electron, heavy hole, and light hole respectively and m_o is the electron rest mass. It should be noted that there is an uncertainty in the electron effective mass at the zone center where fewer experimental studies have been done for silicon.

3.3 Effects of Design Parameters based on Theoretical Calculations

3.3.1 Tunneling Resonance Simulations

In order to understand how the design parameters in the quantum well structure impact the performance, we used tunneling resonance simulations [29, 30] to evaluate their effects in the quantum well energy. The change of exciton binding energy was relatively small and neglected here, and the quantum well energies (i.e., the tunneling resonance energies) as well as Stark shifts of electrons and holes were simulated separately.

The simulation procedure (see, e.g., ref. [62]) includes three steps: (i) first form the potential line-up of the quantum well and divide it into small slices along the growth direction, (ii) build up carrier transfer matrixes for each slice and junction based on the electric field, well/barrier thicknesses, and band alignment as well as carrier effective masses (from the well/barrier compositions), using the parameters in Sec 3.2.2, (iii) multiply the transfer matrixes and then extract the tunneling resonance energy under different electric fields.

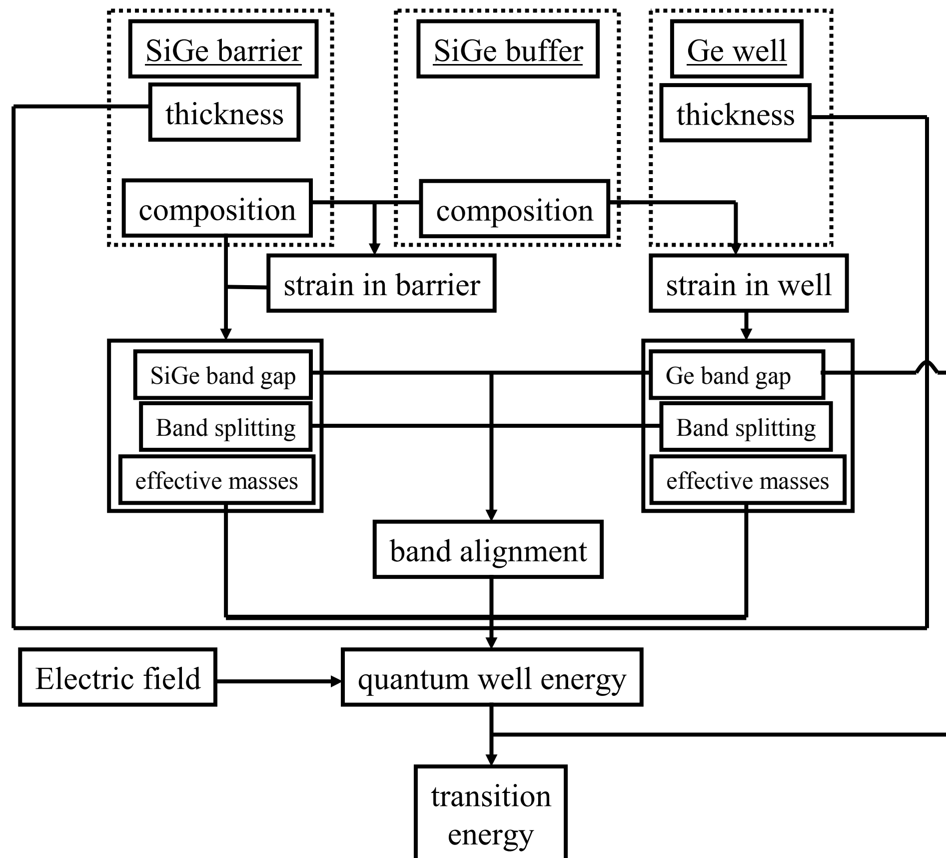

Figure 3.4: Simulation flow and effect of parameters.

The flow of simulations and the effects of design and physical parameters are summarized in Fig. 3.4. Beside this method, the analytical solution, Eq. (2-5), based on the 2nd order perturbation in an infinite quantum well structure also provides more insights into the effects of the well thickness, effective masses, and electric field.

3.3.2 Simulation of Energy Levels and Shifts

Fig. 3.5 shows a typical example of simulated quantum well energies for the electron and heavy hole separately at different electric fields. The initial quantum well energy is dominated by the electron with a light effective mass while the shift is dominated by the heavy hole with a heavier mass. These features are also found in the simulations of different structures and agree with the trends of Eq. (2.2) and Eq. (2.5).

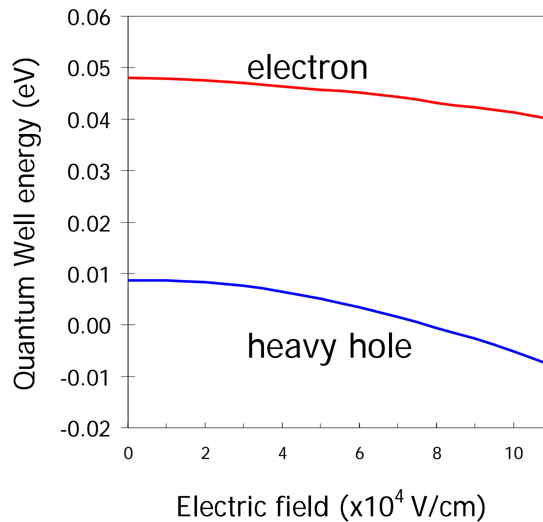

Figure 3.5: A typical simulation of separate quantum well energies of electron and heavy hole at different electric fields. The simulated structure is a strained quantum well, including 10nm Ge quantum well and 16nm $Si_{0.15}Ge_{0.85}$ barrier, on a relaxed $Si_{0.1}Ge_{0.9}$ buffer (collaboration with Y. K. Lee).

The separate quantum well energies of the electron and heavy hole are combined into the quantum well energy, which is lowered with an increased electric field - the Stark effect (i.e., red shift) in the exciton peak and absorption edge. The quantum well

energy and its shift in our strained Ge/SiGe quantum well structure on a relaxed SiGe buffer can be affected by several structure design parameters, including the quantum well thickness, barrier composition and thickness, and buffer composition, as shown in Fig. 3.4. The Ge well thickness is an important design parameter as predicted by Eq. (2.5) based on a quantum well with an infinite barrier height. However, a real quantum well structure cannot have an infinite barrier, thus the barrier height (the offset between the Ge well and SiGe barrier) determined by the barrier and buffer compositions (through the strain effect) would also change the quantum well energy and the behavior of the exciton peaks. The effect of the barrier thickness is negligible here because it is thick enough in a quantum well system to prevent coupling between different wells (though for some specific applications, the coupling between wells and the formation of mini-bands are desired).

Fig. 3.6 shows the electric field dependences of quantum well energy (sum of electron and heavy hole) and exciton shift simulated by the resonance tunneling method with variations in the three key design parameters - the well thickness, barrier composition, and buffer composition - respectively. This result suggests the most important design parameter is the quantum well thickness, which affects the quantum well energy and shift significantly as shown in Fig. 3.6(a). Thin wells have small Stark shifts and high quantum well energies which shift the initial absorption edge (~0.8 eV or 1550 nm for bulk Ge) out of C-band (~1550 nm), and both of these features are undesired here. Thick wells have low quantum well energies and a large Stark shift, which agrees with the analytical model. However, when the wells become too thick, they no longer confine electron-hole pairs and hence the 2-D excitons behave like 3-D excitons, which are easy to ionize and have low absorption efficiency.

Fig. 3.6 (b) and Fig. 3.6 (c) show that the barrier and buffer compositions have weak effects on the well energy and shift. This indicates that SiGe barriers with ~15%

Si concentration provide enough barrier height to confine the electrons and holes inside the wells.

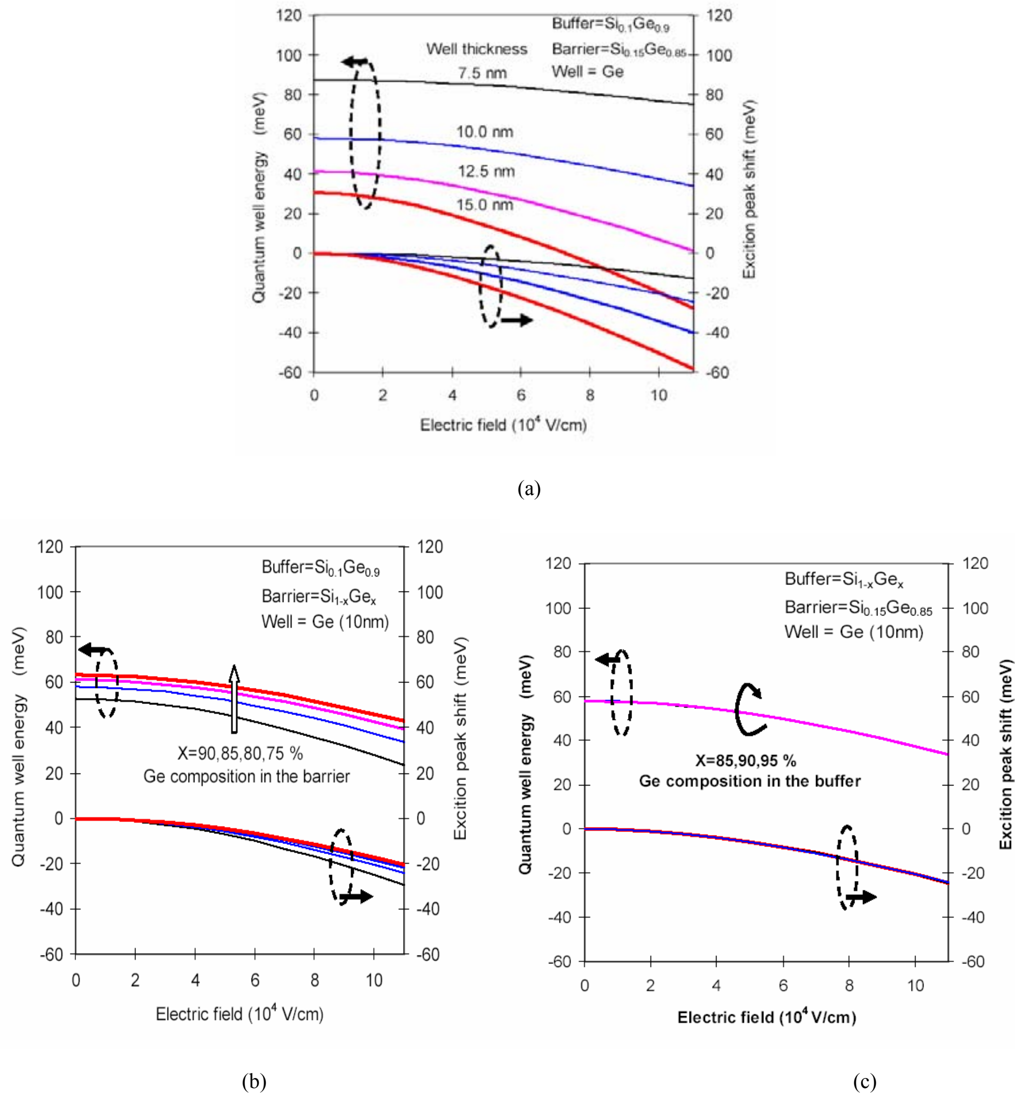

Figure 3.6: Electric field dependence of quantum well energy (sum of heavy-hole and electron) and exciton peak shift (a) with different well thickness (b) with different barrier compositions (c) with different buffer compositions (collaboration with Y. K. Lee).

Besides, there is an assumption used for the conduction band offset as discussed in Sec. 3.2.2. Fig. 3.7 shows the simulated quantum well energies and shifts with

different conduction band offsets (i.e., barrier heights). All three curves are almost identical - a 50 meV change in the offset causes a less than 2 meV variation in the electron energy. The direct band gap energy difference between Si and Ge gives a high direct band gap barrier height in the Ge/SiGe quantum well, and hence the change or uncertainty, if any, caused by this assumption is negligible.

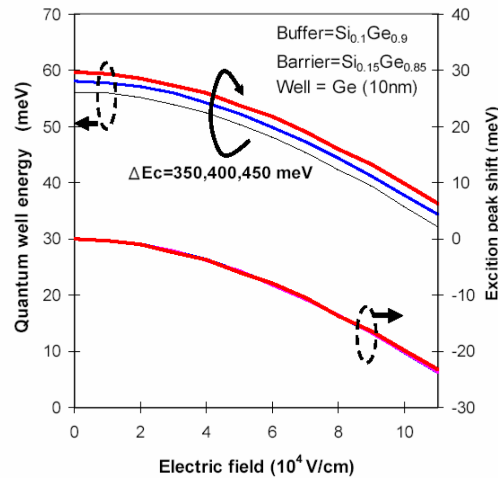

Figure 3.7: Effects of variations in the direct conduction band offset on the quantum well energy with ΔE_c=350, 400, 500 meV (collaboration with Y. K. Lee).

These simulations indicate that the quantum well thickness is the most important design parameter, and the uncertainty in the conduction band offset would not affect the quantum well energy or Stark shift. The comparisons between the theoretical simulations and experimental results will be discussed in Sec 5.5.

Chapter 4 SiGe Material Growth

4.1 SiGe Heteroepitaxy

When the lattice constant of a deposited epi-layer is different from that of the underlying buffer or substrate layer, initially the surface layer is flat and the horizontal lattice spacing is stretched or compressed to match that of the underlying substrate, resulting in the accumulation of elastic strain energy. With increasing increments in both epi-layer thickness and strain energy, the subsequent growth can be divided into three modes, as shown in Fig. 4.1. Each has a different surface morphology: the Frank-van der Merwe mode (layer-by-layer) [63], the Stranski-Krastanov mode (mixed) [64], and the Volmer-Weber mode (island) [65].

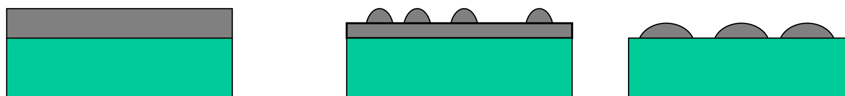

Figure 4.1: Thin film growth modes: (a) Frank-van der Merwe mode (b) Stranski-Krastanov mode (c) Volmer-Weber mode.

The cause of the morphology change is minimization of the combination of the volume energy (the total number and volume of atoms are the same in these three modes, but the energy varies with strain), the bottom interface wetting energy (the first two modes have the same bottom surface energy), and the top surface tension energy

(the most significant variation between 3 different modes). Theoretically the adatom will move to its minimum energy state if it has adequate mobility under equilibrium condition. However, a low substrate temperature or a high growth rate results in non-equilibrium growth which gives a relatively flat surface.

There is a high lattice constant mismatch (4%) between silicon and germanium. Fig. 4.2(a) (and Fig. 4.2(b)) show the atomic structure of a relaxed (and a strained) SiGe epi-layer grown on a substrate with a different lattice constant. If the epi-layer is relaxed and returns to its original crystal structure, the vertical lattice constant will be the same as original one, *a*. If the epi-layer is strained and its lattice spacing is compressed (or extended) to be a_{II} which is the same or close to that of the substrate, its vertical spacing will be extended (or compressed) to $a_{\perp}$.

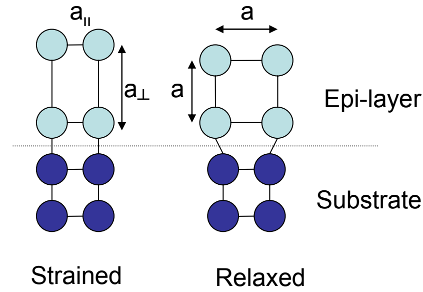

Figure 4.2: Atom arrangements of (a) strained (b) relaxed epi-layer on substrate.

For Fig. 4.2 (a), the stresses on the epi-layer are ε_{II} (parallel to the interface) and $\varepsilon_{\perp}$ (perpendicular to the interface) and can be expressed as

$$\varepsilon_{II} = \frac{a_{II} - a}{a} \tag{4.1}$$

$$\varepsilon_{\perp} = \frac{a_{\perp} - a}{a} = \frac{2\ C_{12}}{C_{11}} \varepsilon_{II}\ , \tag{4.2}$$

where C_{11} and C_{12} are the elastic stiffness constants. C_{11} and C_{12} of Si (and Ge) are 16.58 and 6.39 (and 12.85 and 4.82) respectively (all in units of 10^6 N/cm^2) [66].

4.2 Growth Issues

4.2.1 Lattice Relaxation and 3-D growth

Due to the high lattice mismatch between Si and Ge, the strain energy is high in SiGe heteroepitaxy. When the thickness or composition of the SiGe epi-layer grown on Si exceeds the critical limitation (Fig 4.3(a)) [67-70], the lattice tends to relax by generating dislocations or becomes 3-dimensional (3-D) islands (Fig 4.3(b)) [71]. These problems happen on Si substrates and tend to happen in Ge-rich SiGe at even lower temperatures.

At high temperatures, the growth mode is dominated by 3-D growth. At low temperatures, the adatom mobility decreases, the transformation from 2-D growth to 3-D islands is suppressed, and elastic relaxation is reduced due to decreased dislocation motion. These critical limitations also highly depend on the epitaxy techniques. For a non-equilibrium process (such as MBE and CVD growth), the critical thickness is not constant and decreases with each increment of temperature.

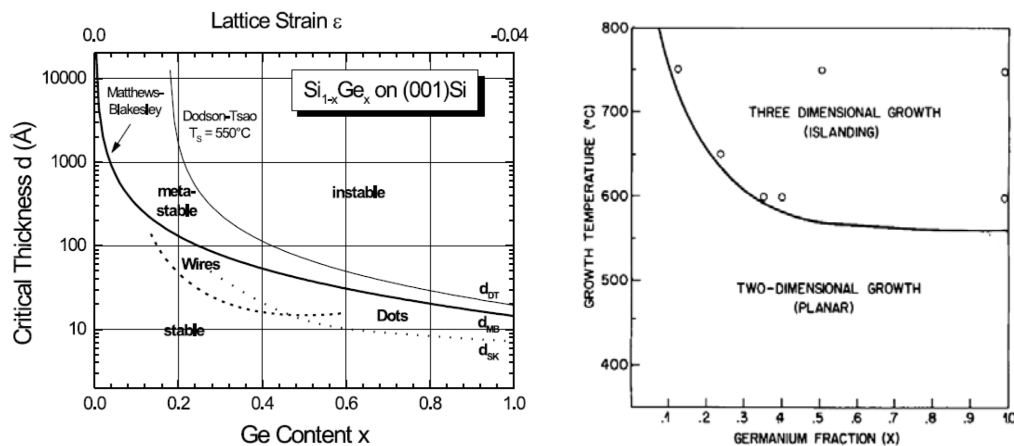

Figure 4.3: (a) Critical thickness of SiGe film on Si [70]. (b) Dependence of growth mode on growth temperature and Ge content [71].

To have a sharp and periodic quantum well structure, a flat surface is necessary and the 3-D growth mode and relaxation should be prevented. However, the relaxation is not always undesired. For example, if a pure silicon layer is grown on a relaxed SiGe layer, the silicon layer will be strained and the two Δ_2 valleys will become the bottom conduction band, which enhances the horizontal electron transport speed (critical for MOS devices) due to the smaller transverse electron effective mass [72]. In our case, in order to control the strain in the Ge/SiGe MQWs, a relaxed Ge-rich SiGe layer is deposited first as an intermediate lattice matching buffer layer. (Another reason is to prevent strain-induced type-II alignment)

4.2.2 Profile Control

The ideal SiGe heterostructure should have precise profile control in the SiGe composition as well as abrupt interfaces, but the diffusion and segregation effects cause transient regions. The segregation is the migration of Ge atoms toward the surface for a lower surface energy, while the diffusion is the exchange of lattice sites between both Si and Ge. These effects usually happen together; however, a sandwich structure shown in Fig. 4.4, i.e., a SiGe layer between the pure Si cap and buffer layers, can be grown to distinguish them. The transition of the Ge fraction in the buffer layer is only affected by the diffusion while that in the cap layer is affected by both diffusion and segregation effects.

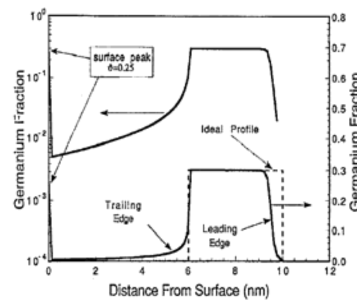

Figure 4.4: Sandwich structure with a larger Ge tail in the trailing edge due to segregation. [73]

4.3 SiGe Epitaxy and Characterization

4.3.1 Epitaxy Tools

The epitaxy tools for this study included molecular beam epitaxy (MBE) [74] and chemical vapor deposition (CVD) systems. The initial material growth was done by MBE, which is the most advanced epitaxial tool for the growth of thin films, nanowires, quantum dots, and for the research of nanoscale phenomena. The knowledge was then applied to CVD growth for its mass-production capability, and the device growths were all done with CVD. Their details will be discussed in Sec. 4.4 and Sec. 4.5.

4.3.2 Material Characterization Techniques

Material characterization techniques used for this study included X-ray diffraction (XRD), secondary ion mass spectrometry (SIMS), Rutherford backscattering spectrometry (RBS), X-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM), atomic force microscopy (AFM), and Hall measurement.

XRD is one of the most important techniques for measurements of the lattice structures and analyses of the strains and compositions of deposited films, especially considering the yield/time efficiency and that it is non-destructive. X-rays are incident onto the crystal plane at a tilted angle and then reflected back into the detector. Since the intensity results from interference between different layers of atoms, the vertical distance of each layer can be extracted from the diffraction pattern. The degree of strain/relaxation in the SiGe heterostructure can then be calculated using the measured vertical lattice spacing information and the epi-layer compositions. In addition, the lattice constant of a deposited SiGe film can be characterized from the peak position of its XRD pattern if it is fully relaxed, and hence the SiGe composition can be known.

The Rutherford spectrum of the backscattered ions is used in RBS to determine the elemental species and thicknesses of thin films. RBS is useful for precise measurements of SiGe compositions and can provide calibrated samples as standards for SIMS measurements. SIMS can measure the SiGe compositions and dopant concentrations of films, and it has a higher sensitivity and good depth profiling ability; however, the atom masses of Ge and As are close, thus it is relatively difficult to measure low-level As dopant concentrations in SiGe samples. XPS, also called electron spectroscopy for chemical analysis (ESCA), measures the binding energies and chemical shifts of the peaks to determine the composition in the sample surface, and it has a relatively lower resolution than SIMS. TEM can provide both real-space and reciprocal-space lattice images of SiGe samples with the highest resolution to study the structure, composition, defects, and crystal phase; however, its sample preparation is very delicate and time consuming. AFM probes the sample surface with a vertical resolution finer than an atomic layer, and the scanned surface morphology is useful to determine the growth mode. Hall measurements characterize the carrier mobility at different temperatures, and its temperature dependence is used to determine which mechanism dominates the scattering process. The mobility is also the most important criterion in evaluating the electrical design of SiGe structures.

4.4 Molecular Beam Epitaxy (MBE)

4.4.1 MBE System

The MBE system used here was a modified Varian GEN-II system (shown in Fig. 4.5), which was converted from a III-V epitaxy chamber into a group-IV chamber for SiGe epi-layer and Si nanowire growth. It contains three main chambers – a load chamber, a transfer chamber, and a group-IV growth chamber - and is connected to another III-V

MBE system through the transfer chamber. The load chamber can accommodate up to twelve wafers and has a base pressure of 10^{-3} Torr. The base pressures of the transfer and growth chamber are in the ranges of 10^{-9} Torr and 10^{-11} Torr, respectively. The three-stage design provides a buffer effect to slow the pressure rise during the transfer of wafers between different chambers as well as to reduce the burden on the pumps.

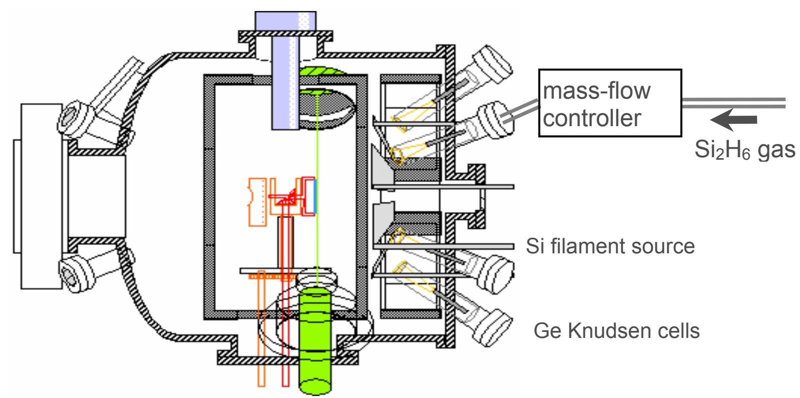

Figure 4.5: schematic of a MBE system with Si and Ge sources.

The ultra-low growth chamber pressure minimizes contaminants and prevents the collision of the evaporated atoms or molecules, resulting in a long mean-free-path, line-of-sight growth. After reaching the surface of the substrate, the source atoms or molecules undergo absorption, deformation, migration processes, and form chemical bonds with surface atoms as well as reorder the crystal structure at the surface. MBE growth is determined by the surface kinetics, so it is a non-equilibrium process while the liquid phase epitaxy (LPE) is a quasi-equilibrium process. MBE can achieve precise control of the vertical composition and doping profile on an atomic-layer scale with excellent lateral uniformity.

The growth chamber includes beam generators, shutters, beam and growth monitors, and a substrate holder/heater. The beam generators in our system include a silicon filament source, a germanium effusion Knudsen cell (K-cell), a titanium

filament source (for the nanowire catalyst deposition), a disilane (Si_2H_6) injector as the gas silicon source, and two doping sources, boron and arsenic, for p-type and n-type dopants. The beams are interrupted by their shutters except the disilane source which is controlled by a mass flow controller (MFC). Monitor equipment includes reflection high energy electron diffraction (RHEED), ion gauge, and quadruple mass analyzer. RHEED is a powerful in-situ tool to monitor the reciprocal crystal structure of the top surface epi-layer and to check whether it is single crystal, poly, or amorphous. Also oscillations of the RHEED pattern can be used to count the number of grown atomic layers. The ion gauge can measure the beam flux from each source, and the quadruple mass analyzer can measure the residual gas in the chamber. The substrate holder holds the substrate wafer and rotates it during the growth for growth uniformity, and on the back, a heater and thermocouple control the growth temperature.

4.4.2 Substrate Preparation Procedure

Si substrate: Before loading, silicon wafers receive a non-standard pre-deposition clean in the Stanford Nanofabrication facility (SNF) lab. They are dipped in 4:1 H_2SO_4:H_2O_2 at 90ºC for 10 min, 5:1:1 HCl:H_2O_2:H_2O for 10 min at 70ºC, 2% HF for 30 s, and 5:1:1 HCl: H_2O_2:H_2O again for 10 min, with a 6-cycle de-ionized (DI) water dump/rinse between each step, and finally spin-dried. The final HCl (instead of HF) dip forms a thin oxide protective layer on the substrate surface, and hence contaminants introduced during the wafer transfer do not get into the silicon wafers. The cleaned wafers are loaded into the load chamber and baked at 200ºC for 60 min, and then they are kept in the transfer tube before and after growth. During growth, the wafer is loaded into the growth chamber and baked at 850ºC for 30 min to desorb the chemical oxide (at the same time, any surface containment is also desorbed), and then a thin silicon buffer layer is deposited using the gas silicon source before the growth of device layers. If the wafer is not clean, the grown buffer film will contain many cone-

shaped pits, which are hundred nm wide and visible under scanning electron microscope (SEM).

Ge substrate: After removal from the package, each Ge wafer is cleaned individually. It is cross-dipped between DI water, H_2O_2, and HCl – H_2O_2 oxidizes the surface of Ge to form GeO_x while HCl etches the GeO_x [75]. This procedure is repeated to form and etch GeO_x, to remove several surface atomic layers of Ge as well as any residual contaminant. Another way to form the surface GeO_x layer is ultraviolet(UV)-ozone oxidation [76]. The wafer is baked in the load chamber at 200 ºC for 60 min and then loaded into the growth chamber and baked at 600 ºC for 30 min to desorb the surface oxide.

***GaAs* substrate:** GaAs wafers can be directly loaded into the system and baked in the load chamber without special cleaning. Before the growth of SiGe structures, a 0.2~0.5 μm GaAs buffer layer is grown in another III-V chamber at 650ºC with a 15 times As-to-Ga flux ratio.

4.4.3 Growth Control and Calibration

The doping level and composition of epitaxial layers are determined by the source materials, flux ratios, temperatures, and growth interruptions. The use of shutter interruptions is a very important and unique technique in MBE to produce sharp profiles because it stops the growth and leaves time for lattice reordering and the formation of the smoothest surface, whose correspondence in k-space is the maximum of the RHEED intensity.

During the calibration growth (after every opening or several months), the source flux of each element is measured by an ion beam gauge, and the respective concentration and thickness of the calibration sample are measured by ex-situ RBS and SIMS. The extracted growth rate is correlated to the respective beam flux, and

hence the growth profiles can be controlled by only changing the source temperatures and calibrating their fluxes before each subsequent growth.

4.4.4 SiGe Growth

The Ge effusion cell and both gas and solid silicon sources were used to grow SiGe films by MBE. The growth rate of Ge was varied from 0.1 to 10 nm/min with the source temperature ranging from 1100 to 1300 ºC. For solid source silicon deposition, the silicon filament was heated to 900-1000 °C to yield a growth rate between 1-10 nm/hr. The disilane gas source provides a much higher growth rate, which depends on the substrate temperature and its partial pressure in the chamber. Its operation is more like CVD and there are more restrictions in the growth optimization. After arriving at the substrate surface, disilane molecules are decomposed into silicon and hydrogen. The hydrogen atoms terminate the Si surface dangling bonds and reduce segregation of germanium or dopant atoms from the substrate to the surface.

4.4.4.1 SiGe on Si Substrates

Before the growth on Si, a pure Si buffer layer was deposited using 2.5 sccm disilane at 700 °C with a growth rate of 5 nm/min. The growth techniques for the subsequent layers depend on the structures.

Delta SiGe layer: The bottom and cap Si layers were deposited from the disilane source using the same growth conditions as the Si buffer. The delta SiGe layer was grown using both solid Si and Ge sources at a low temperature, normally 300-350°C. The solid sources give precise growth rate control for the delta layer, and a low substrate temperature is preferred to prevent the diffusion and segregation of Ge.

Thick and relaxed SiGe layer: In order to get a reasonable growth rate, disilane silicon was used with a solid Ge source. During the growth, the Ge flux was kept constant, and the growth temperature ranged from 500 to 700 °C, depending on the

required growth rate and composition of the SiGe layer. In this case, the disilane can prevent Ge segregation, but not diffusion, so the transition region of the leading edge is relatively broader.

***3-D growth**:* The deposition of Ge on Si at a high temperature is useful for quantum dot growth. If the strain energy accumulation and substrate temperature are high enough, the surface adatoms have sufficient kinetic energy to diffuse and form dome or pyramid structures [70], and the growth mode will become 3-D islanding. RHEED was used to monitor this behavior. During the Si buffer growth, RHEED oscillations were stable, and the RHEED pattern showed a combination of (2x1) and (1x2) reconstructions. When the Ge or Ge-rich SiGe layer was deposited on Si, the RHEED intensity immediately decreased and the pattern finally became spotty, which reflects the change of growth from a 2-D layer to 3-D clustering.

4.4.4.2 SiGe on Ge and GaAs Substrates

The 4% lattice mismatch between Si and Ge creates a challenge to the growth of thick strained SiGe layers. It can induce misfit dislocations and 3-D islanding to relieve the strain. To prevent these problems in MBE growth, Ge-lattice-matched substrates (pure Ge or GaAs wafers, which are acceptable in the MBE chamber) were used to grow Ge-rich SiGe films with solid Ge and Si sources. The growth study was carried out at low growth temperatures ranging from 250 to 450 °C. In-situ RHEED showed the samples grown below 300 °C have less streaky patterns and low crystal quality.

The strain was confirmed by XRD. Fig. 4.6 shows the XRD patterns of 100nm $Si_{0.2}Ge_{0.8}$ films on GaAs. The fully-strained sample grown at 350 °C is perfectly matched to the curve of the theoretical simulation, while the 400 °C film has a broader and asymmetrical peak.

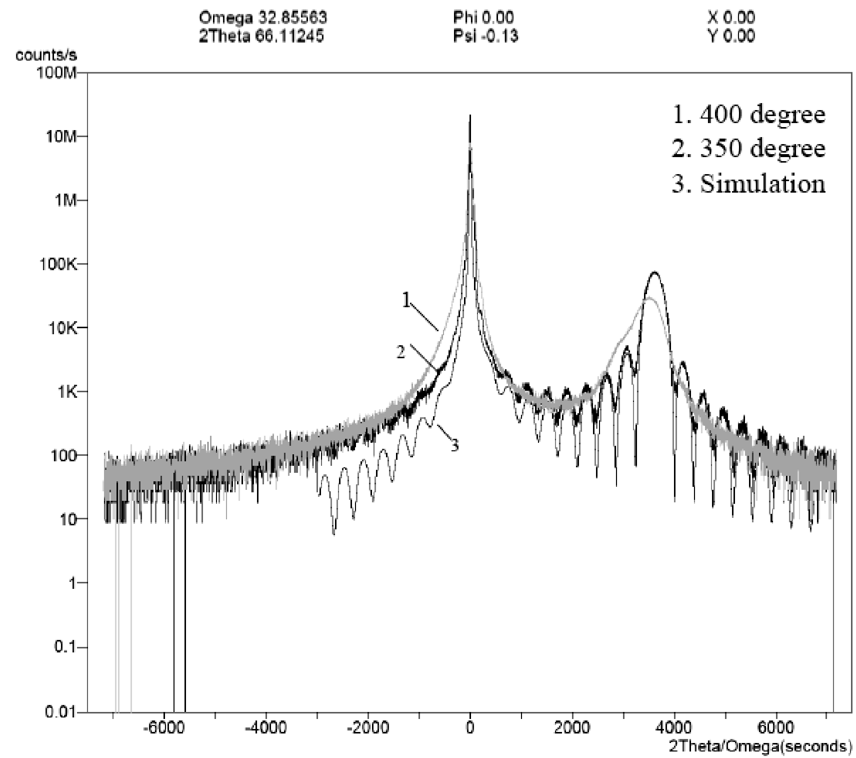

Figure 4.6: Strain analysis of MBE-grown SiGe films on GaAs by XRD.

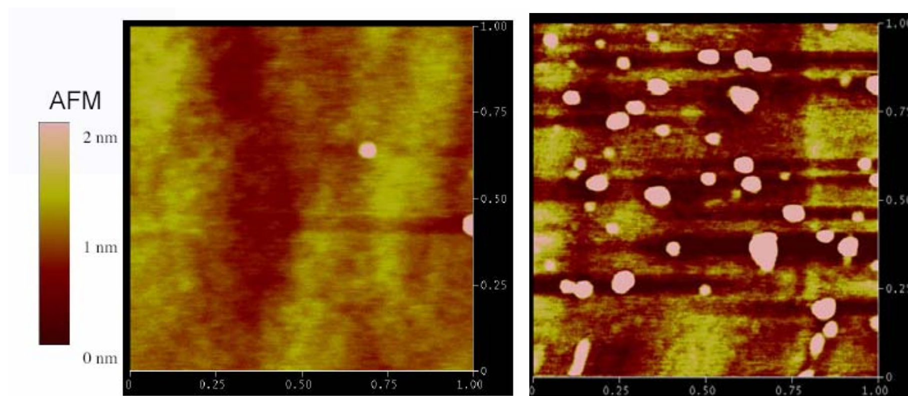

Figure 4.7: AFM images of SiGe-on-Si grown at (a) 350ºC (b) 400ºC.

AFM images (Fig. 4.7) show 3-D islanding happens when the growth temperature exceeds 400°C. The optimal growth temperature is 350 °C. If the disilane gas is

injected into the growth chamber during the solid-source growth, it reduces the surface hopping sites and suppresses the surface roughness as shown in Fig. 4.8.

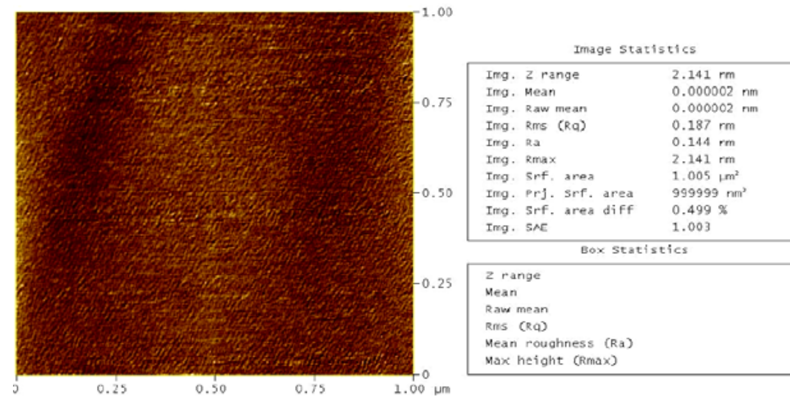

Figure 4.8: AFM image of SiGe-on-Si grown at 350ºC by solid sources with disilane in the chamber. The root-mean-square (RMS) roughness is less than 0.2 nm.

4.4.4.3 QW Growth and Sharpness Control in MBE

The lower surface energy and high surface mobility of Ge normally cause severe diffusion and segregation problems in SiGe growth - this happens during SiGe growth on Si, and it also occurs on Ge, but at a much lower temperature. The Ge/SiGe QW grown by closing/opening the Si source shutter has an asymmetrical profile, which has a smoother trailing edge and an abrupt leading edge - a typical signature of Ge segregation. To eliminate this effect, a gradient in SiGe composition is produced by ramping the flux ratio between Si and Ge to achieve a symmetric profile.

4.5 Chemical Vapor Deposition (CVD)

4.5.1 CVD System

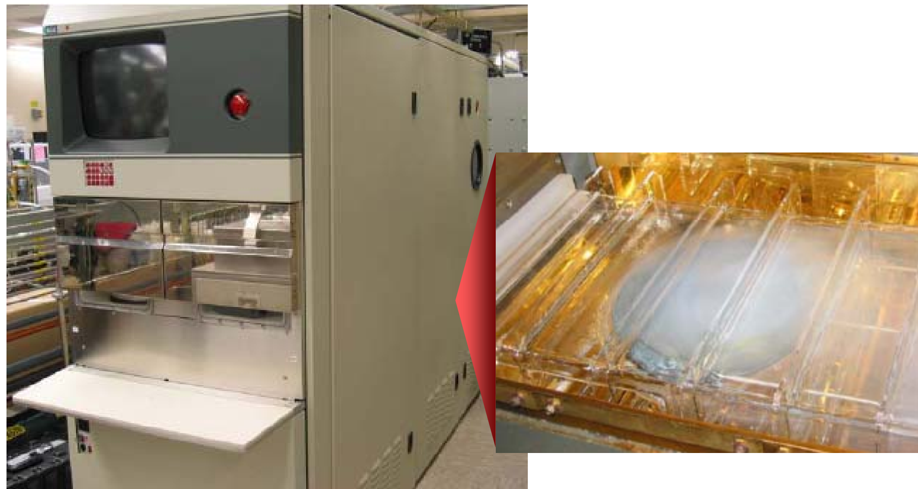

Figure 4.9: ASM RPCVD reactor used for this study.

The CVD tool used for this study was a reduced pressure CVD (RPCVD) reactor. It is a commercially available, cold-wall, single-wafer, mass-production tool and is routinely used in CMOS chip fabrication processes. The model here was an ASM Epsilon II reactor shown in Fig. 4.9. The base pressure is 0.45 mTorr with 15 mTorr/min leak rate. The growth pressure ranges from ~10 Torr to 760 Torr.

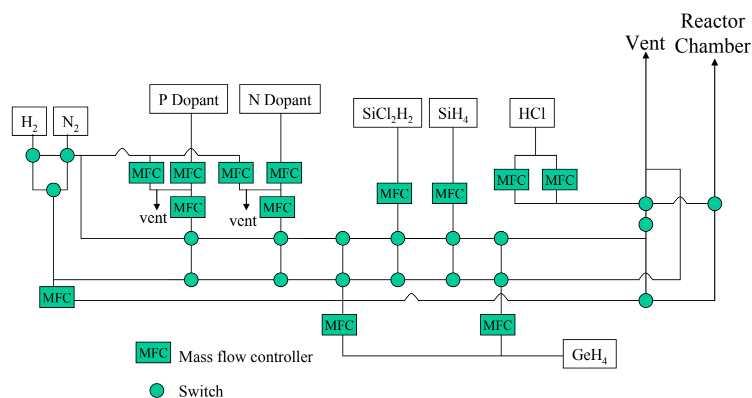

Figure 4.10: Schematic of gas flow control.

The schematic of the gas control panel is shown in Fig. 4.10. The gas precursors include silane (SiH_4) and dichlorosilane (DCS) for Si, germane (GeH_4) for Ge, as well as diborane (B_2H_6), arsine (AsH_3), and phosphine (PH_3) for dopants. The carrier gases are hydrogen and nitrogen, and the etching gas is HCl.

4.5.2 Growth and Calibration

Before loading, the Si wafers are cleaned in the standard pre-deposition procedure (4:1 H_2SO_4:H_2O_2 at 90ºC for 10 min, 5:1:1 HCl:H_2O_2:H_2O at 70ºC for 10 min, 2% HF for 30 s, with DI water dump/rinse between each step, and finally spin dried). No extra protective layer is necessary because the cleaning bench and the epi reactor are in the same SNF lab.

After loading the wafers, the load chamber is nitrogen-purged. Before each growth, the growth chamber is HCl etched to remove any prior residual SiGe film and dopant atoms. Prior to growth, the Si substrates are baked at 1150 ºC for 5 min, and then epi-layers are grown by custom recipes edited by growers. Wafers are unloaded after the growth and sent for characterization and processing.

The composition of the SiGe calibration sample was measured by RBS and the result was used to calibrate the SIMS measurement. The thickness and composition of any SiGe film deposited afterward can then be measured by SIMS. Fig. 4.11 shows a series of SiGe layers deposited on Si at the same temperature with different gas fluxes. The growth rate can be extracted by dividing the thickness of each layer over its growth time.

The thickness of epitaxial layers can also be characterized by SEM, TEM, and mass-difference. SEM and TEM can show real cross-sectional images of the deposited SiGe film, which provide the most accurate thickness measurement if the sample is well aligned and the cross-section is parallel to the growth direction. The mass-

difference method uses a scale to measure the mass increment after the deposition of a single SiGe layer. When the SiGe density (i.e., composition) as well as the wafer size are known, the thickness can be calculated by dividing the mass difference over the wafer surface area and film density. The accuracy is 5~10 nm, so the deposited film thickness should be at least 0.5µm. It shows a consistency when comparing the values of the same wafers before cleaning and after cleaning/baking (without growth). The results are also compared and correlated to the SIMS and TEM measurements. This method is convenient because it is a quick, non-destructive, and accurate method to calibrate a single, thick, known-composition SiGe layer on Si.

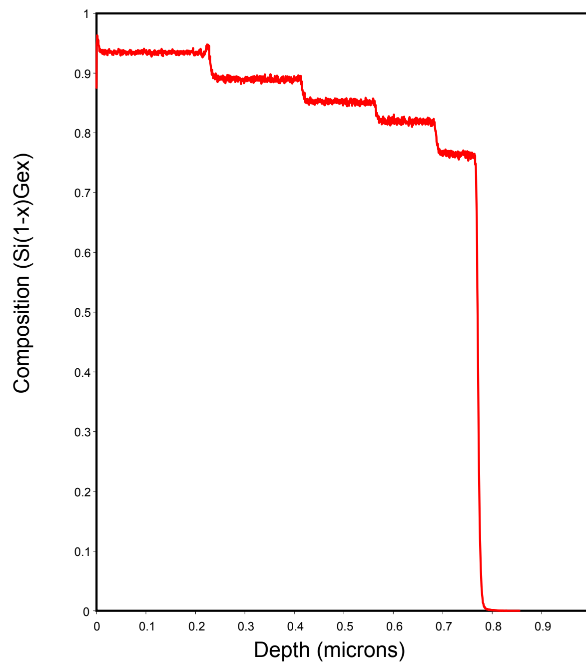

Figure 4.11: SIMS measurement of SiGe step layers grown on Si by RPCVD.

4.5.3 SiGe Growth Rate

There are five growth parameters, including the germane flux, silane flux, carrier gas (H_2) flux, chamber pressure, and growth temperature, which determine the SiGe

composition and growth rate. The growth rate study here was mainly focused on Ge-rich SiGe films grown on [100]-oriented silicon wafers at ~ 400ºC. It is found that when the germane and silane fluxes as well as the growth temperature are fixed, the growth rate of SiGe (with 5% Si content or more) and pure Ge are both inversely proportional to the carrier gas flow, however, the former is almost independent of the chamber pressure while the later is proportional to it.

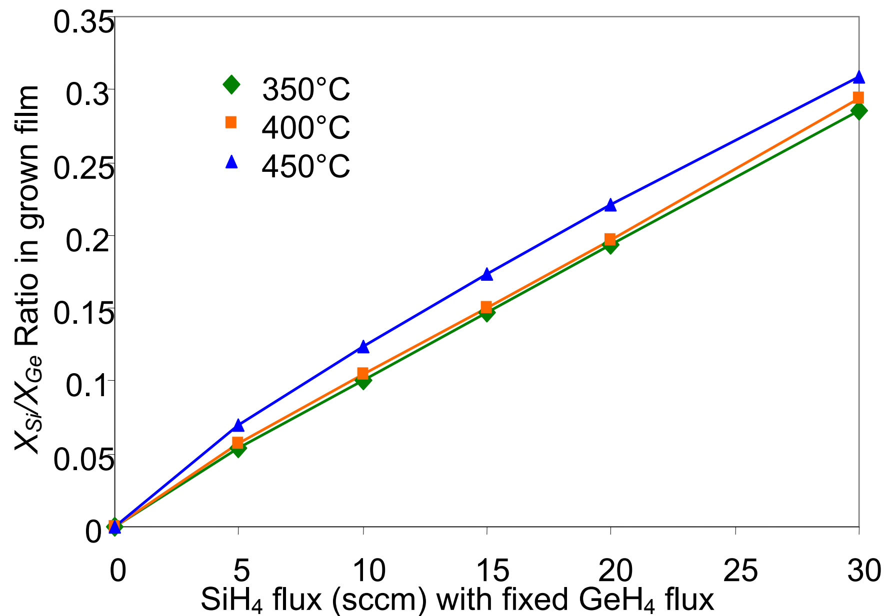

Figure 4.12: Concentration ratios between Si and Ge versus silane flux over a 30sccm flux range with a fixed 30sccm germane flux at different growth temperatures.

A series of SiGe samples were grown at different temperatures (350, 400, and 450 ºC). The germane flux, hydrogen flux, and chamber pressure were 30 sccm, 40 lpm, and 40 Torr respectively, and the silane flux was varied from 5 to 30 sccm. The SiGe growth rate (R_{SiGe}) and composition (X_{Si}, X_{Ge}) with the respective silane flux were extracted from SIMS measurements. Fig. 4.12 shows the concentration ratio (X_{Si}/X_{Ge})

versus the silane flux at different growth temperatures. The SiGe concentration ratio is proportional to the Si/Ge flux ratio, but almost independent of the growth temperature. The growth rate of Ge, R_{Ge}, can be deduced from the total SiGe growth rate and Ge concentration. Fig. 4.13 shows the log of growth rate of Ge ($\log(R_{Ge})$) versus the Si concentration (X_{Si}) at different temperatures. The growth rate increases with a higher growth temperature but decreases with a higher silicon concentration. It is interesting that $\log(R_{Ge})$ at the same temperature has a linear dependence on the SiGe composition.

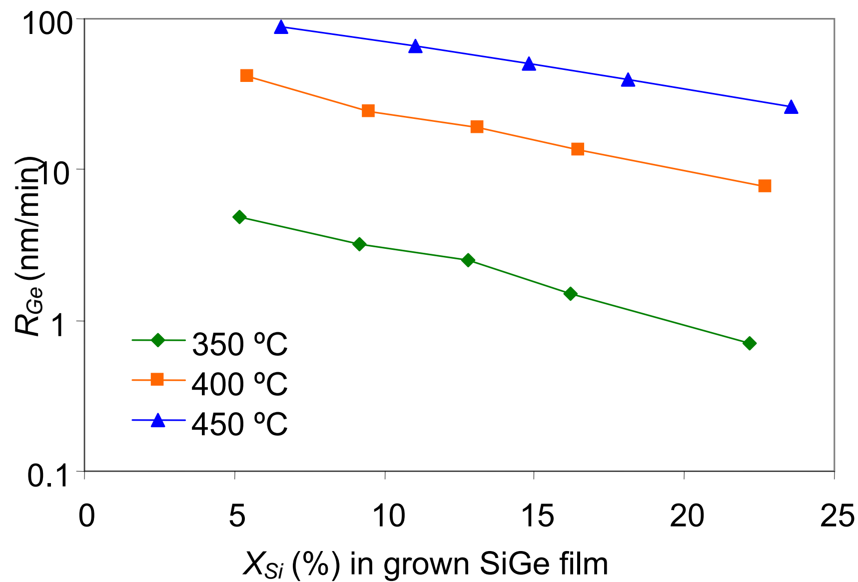

Figure 4.13: R_{Ge} (in log scale) versus Ge content at different growth temperatures. R_{Ge} is the growth rate of the Ge portion in SiGe films.

4.5.4 SiGe Growth Model

The growth of SiGe includes several stages: gas transportation and diffusion onto the surface, absorption or sticking of hydride molecules on the surface, desorption of hydrogen atoms, and adatom movement to the appropriate step-edge sites. A

simplified model is shown in Fig. 4.14(a), and the chemical reaction processes are shown in Fig. 4.14(b) [77, 78]. The growth rate is limited by the transportation at high growth temperatures and by the surface reaction rate at low growth temperatures.

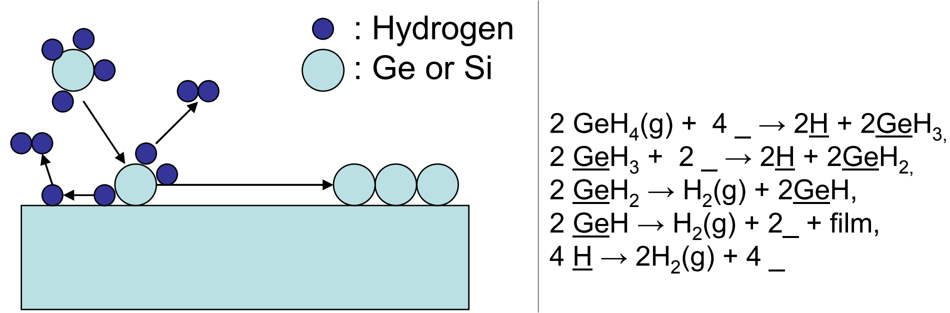

Figure 4.14: (a) Simple growth model. (b) Chemical reaction processes.

If the surface fraction of hydrogen-occupied sites is Θ, P_{Si} and P_{Ge} are the partial pressures of silane and germane in the growth chamber, and k_{Si} and k_{Ge} are the absorption rate constants for silane and germane, then the growth rate of Si and Ge can be expressed as [77]

$$R_{\mathrm{Si}} = 2\ k_{Si} P_{Si} (1-\Theta)^2 \tag{4.3}$$

$$R_{\mathrm{Ge}} = 2\ k_{Ge} P_{Ge} (1-\Theta)^2 . \tag{4.4}$$

Since the hydrogen desorption from surface Ge atoms is faster than from Si atoms, the silane decomposition rate and silicon growth rate (R_{Si}) highly depend on the diffusion and desorption of hydrogen to the nearby Ge atom, especially for Si-rich SiGe growth. However, the Ge-rich (X_{Ge}> 70%) films studied here make the absorbed silane being surrounded by at least three Ge atoms directly, so the hydride decomposition is relatively independent of the Ge concentration. When Eq. (4.3) is divided by Eq. (4.4) into

$$\frac{R_{Si}}{R_{Ge}} = \frac{k_{Si}}{k_{Ge}} \cdot \frac{P_{Si}}{P_{Ge}} , \tag{4.5}$$

which explains why the Si and Ge concentration ratio of the grown films is proportional to the gas flux ratio, but independent of the growth temperature for a specific range (as shown in Fig. 4.12) when the ratio of absorption rate constants (k) is also independent of temperature in this temperature range. Similar results are also found in the SiGe growth by ultra-high-vacuum CVD (UHV-CVD) using germane and disilane [79].

The log of Eq. (4.4) can be expressed as

$$\log(R_{Ge}) = \log(k_{Ge}) + 2\log(1-\Theta) + \log(2P_{Ge})\,. \qquad (4.6)$$

Considering (i) $\log(R_{Ge})$ has a linear dependence on the SiGe composition (shown in Fig. 4.13), (ii) P_{Ge} is fixed at 30 sccm, and (iii) a near zero Θ is assumed (the surface atoms are mainly Ge with a high desorption rate, thus the unoccupied surface fraction is high here), so $\log(k_{Ge})$ should also have a linear dependence on the SiGe composition. Since $\log(k_{Ge})$ is proportional to the activation energy, this dependence can be explained by a linear composition dependence of the activation energy.

4.5.5 Doping Control

There are four different dopant sources, including 1% B_2H_6 (for high p-doping), 100 ppm B_2H_6 (for low p-doping), 1% PH_3 (for high n-doping), and 100 ppm AsH_3 (for low n-doping), available for this study. Their growth mechanisms are similar to Si and Ge hydride. The use of high-level PH_3 or B_2H_6 during the SiGe growth can change the growth rate but not affect the SiGe composition more than 1%. Here only the buffer and cap layers are doped (lightly by using low-level B and As sources) in real devices, and the composition control in these layers is more important than the thickness control, so the change of SiGe growth rate, if any, caused by the addition of dopants would not affect devices. The activation of dopants and electrical doping levels can be evaluated from the carrier concentrations measured by the Hall set up.

4.6 SiGe Buffer Growth

4.6.1 Comparison of SiGe Buffer Methods

In order to control the strain in Ge/SiGe quantum wells, Ge-rich SiGe buffer layers are grown on Si substrates in the design of Sec. 3.1. The commonly practiced methods of SiGe buffer growth are shown in Fig. 4.15, including: the graded buffer method, the direct buffer method with single-growth-temperature, and the direct buffer method with two-growth-temperatures. For the graded buffer method, the Ge concentration of the SiGe layers grown from pure Si substrates keeps increasing from zero to the final composition. It can be linear-graded with a continuous concentration change or step-graded with discrete concentration jumps. For the direct buffer method, films with a single SiGe composition or pure Ge are deposited on top of silicon substrates. The growth is done at either the same temperature or two (low, and then high) temperatures. After growth, the wafers are annealed at higher temperatures. The procedure can be iterated several times.

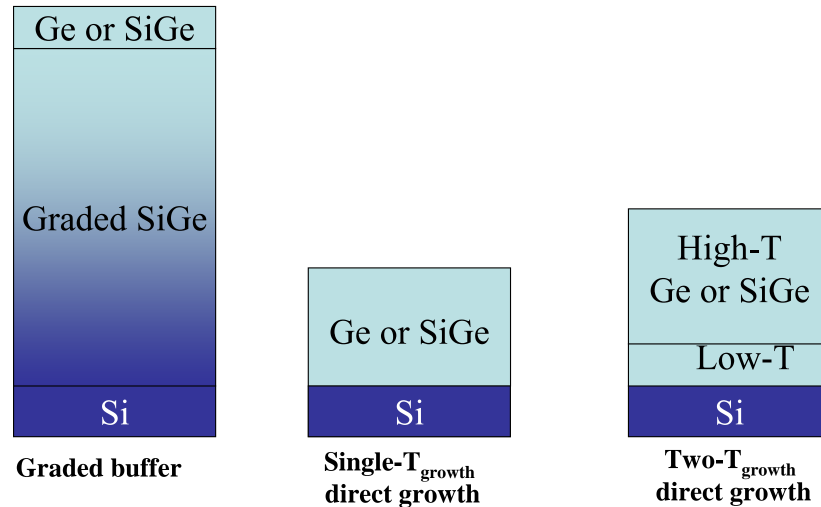

Figure 4.15: Buffer growth methods: (a) graded buffer (b) direct buffer with single growth-temperature (c) direct buffer with two growth-temperatures.

Method	Graded buffer		Direct buffer		
			Two-temperature growth	Single-temperature growth	
Epi-tool (reference)	UHV-CVD [83]	MBE [84]	UHV-CVD [86], MBE [87], RPCVD [88]	MBE [85]	RPCVD [89]
Procedure	Graded $Si_{1-x}Ge_x$ from x = 0 to 100%		two-temperature growth (low/high), high-T anneal (cyclic)	Grow above melting temp	Low-T growth, high-T anneal (multi-cycle)
As-grown Roughness	High	Low	Flat	High	High
Roughness reduction method	CMP at $Si_{0.5}Ge_{0.5}$	Sb Surfactant	Not necessary	Not used	Annealing
TDD (cm^{-2})	$2.1x10^6$	$5.4x10^5$	> 10^7	1~3 x 10^5	10^7
Thickness	10 µm	4 µm	1 µm	2.5 µm	0.4~1 µm

Table 4.1: Comparison of Ge-on-Si growth methods. [83-89]

In the Ge-rich SiGe buffer growth, most studies were targeted to the pure Ge-end for laser, photodetector, and electronics applications based on Ge-on-silicon or III-V-on-Ge-on-Si [80-82]. Here we compare several growth methods of Ge-on-Si buffers from the literature and summarize them in Table 4.1. It should also be noted that our buffer layer is Ge-rich SiGe, not pure Ge.

In graded buffer methods, one well known example is the combination of graded buffer with chemical mechanical polishing (CMP) [83]. A 12-µm linearly graded SiGe buffer layer was grown by UHV-CVD with a 5%/µm Ge grading rate. A chemical-mechanical polishing (CMP) step was used at the intermediate layer ($Si_{0.5}Ge_{0.5}$) to smooth the rough cross-hatched surface. Another example was an MBE-grown SiGe buffer with an antimony (Sb) surfactant to suppress the surface roughness and to help the movement of misfit dislocations which relieve the strain and reduce the generation of threading dislocations [84]. The main drawbacks of graded buffer methods are the

thick buffer layer and extra treatments to suppress the surface roughness. Their key advantage is the resulting lower threading dislocation density (TDD).

In direct growth of Ge on Si, one interesting way was to deposit Ge on Si above the Ge melting temperature [85]. This achieves the lowest TDD, but with very rough surfaces. Since real device applications require flat surfaces, the key is to suppress the surface roughness (3-D islanding) caused by the high mismatch between Si and Ge. Several methods were: (i) Two-growth-temperature method (two-step growth) [86-88]. The deposition of a ~30-50 nm Ge layer on the Si substrate is done at a low temperature (300-350 ºC) to keep the layer flat and relaxed (by generating threading and misfit dislocations instead of by 3-D islanding), followed by deposition of a thick Ge layer at a high temperature (~600ºC), which does not suffer from strain and 3-D growth problems (since the Ge layer below is already relaxed) and also has a high crystal quality. Then the film is annealed at even higher temperatures (800-900 ºC) to reduce the TDD. (ii) Single growth-temperature method (multiple hydrogen annealing for heteroepitaxy, MHAH) [89]. Ge is directly grown on Si at a relatively high temperature (~400 ºC) and then annealed at high temperatures to reduce the surface roughness and TDD. The initial surface roughness is so high that the annealing step reflows the atoms and improves the surface roughness (for other Ge-on-Si cases, the high temperature annealing step usually increases the surface roughness). This requires several cycles of growth/annealing. The drawbacks are the high initial surface roughness and the need of long-time annealing at a specific high temperature range to reduce the roughness. Both methods can achieve a moderate TDD level (~10^7/cm^2), and the roughness in (i) is lower than (ii), but it requires two growth temperature steps.

Comparing all these Ge-on-Si methods, it is obvious that there exist trade-offs between material merits – the required buffer thickness, surface roughness, and threading dislocation density. Because the surface roughness is more critical than

TDD for our quantum well devices, we prefer the direct growth method with less surface roughness.

4.6.2 Direct SiGe Buffer Growth

Our SiGe buffer growth requires a flat surface and thin layer. Since the QCSE is based on absorption which is not affected by threading dislocations, a moderate TDD is acceptable. A thin buffer is preferred to ease the optical design and improve the growth yield. In addition, the SiGe growth rate and composition at two different temperatures might vary dramatically; in order to keep the same SiGe composition in the buffer layer, growth should be done at the same temperature.

4.6.2.1 Surface Morphology

The key difference between the Ge-rich SiGe and pure Ge depositions on silicon is that the Si atoms in the SiGe films can suppress the 3-D growth. A flat initial surface can be achieved in the SiGe-on-Si growth at a single-growth-temperature, but the pure-Ge-on-Si growth requires annealing to reduce the roughness or two growth-temperature stages.

Fig. 4.16 shows two AFM images of Ge-on-Si and SiGe-on-Si samples. The Ge-on-Si sample was grown by MBE using the two-growth-temperature method (300/600ºC), so it had only 0.2 nm root-mean-square (RMS) roughness as shown in Fig. 4.16(a) – an extremely flat surface with obvious atomic-step contours. It represents the best as-grown surface in the Ge-on-Si case. The SiGe-on-Si sample was grown by RPCVD at a single growth temperature (400ºC). The silicon concentration is only 10%, but the initial RMS surface roughness is also only 0.2 nm as shown in Fig. 4.16(b) while that of pure Ge-on-Si growth with the similar condition is 25 nm. This proves silicon can improve the surface morphology. After annealing, the surface roughness increases to 1~2 nm with longer annealing time and higher temperature.

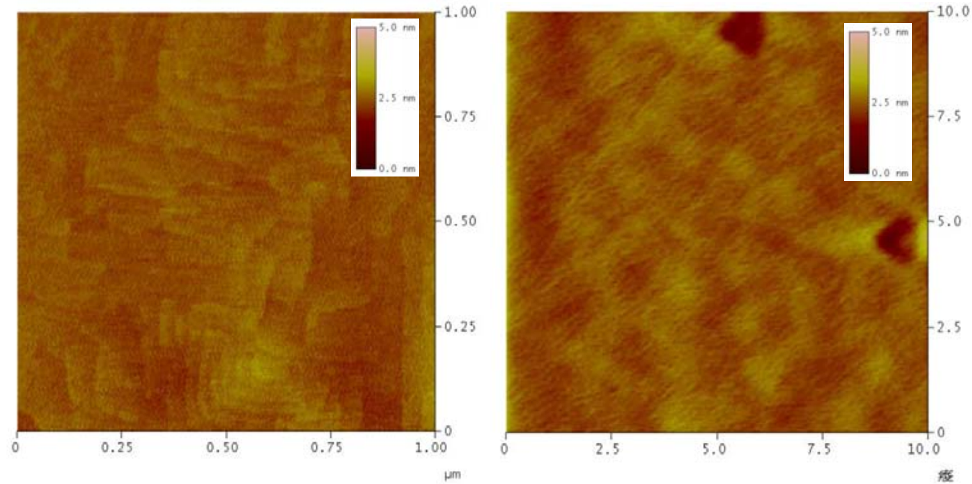

Figure 4.16: AFM image of as-grown surface. (a) MBE-grown Ge-on-Si with 2-growth-temperature (b) RPCVD-grown SiGe-on-Si at single growth temperature.

4.6.2.2 Threading Dislocations

Fig 4.17 shows a cross-sectional TEM image of annealed $Si_{0.05}Ge_{0.95}$ on Si. First a SiGe layer was deposited on silicon and then annealed at 850 ºC, and then another SiGe layer was deposited to observe the propagation of dislocations. It is clear that most threading dislocations are near the Si-SiGe interface and confined inside the first layer, so few dislocations propagate into the 2nd layer in this 4.5 μm section. But it should be noted that there are still threading dislocations penetrating through the buffer in other places, this image just proves most dislocations are confined in the first layer. Though threading dislocations would increase the dark current density, this is not a serious issue for the modulator device operation because the signal is carried by the intensity of light being absorbed, not the photocurrent. Also, the long term reliability issue caused by threading dislocations is less severe in SiGe devices than in III-V devices [90], owing to the higher energy requirement for Si and Ge atom movements and the lower energy imparted into the lattice by a non-radiative recombination of an electron and hole.

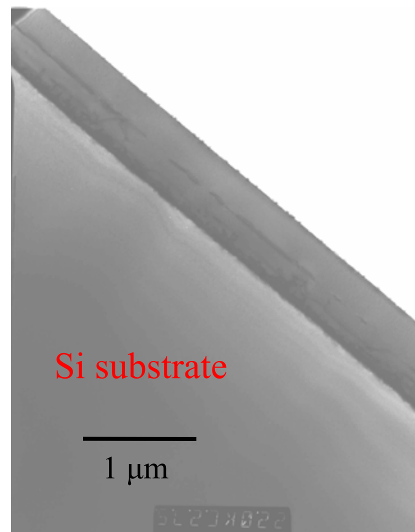

Figure 4.17: Cross-sectional view TEM image of SiGe-on-Si. Two SiGe layers are deposited on the Si substrate with an annealing step before the second layer's deposition. The span of the SiGe film shown here is 4.5 μm.

4.7 Ge/SiGe Quantum Well Structure Growth

4.7.1 Strain-Balanced Structure Design

Fig. 4.18 shows the strain balance in the MQW structure design proposed in Sec. 3.1. Above the relaxed $Si_{1-z}Ge_z$ buffer layer, the Ge wells and SiGe barriers are strain-balanced. Since the Ge well is definitely compressively strained relative to the $Si_{1-z}Ge_z$ buffer, the $Si_{1-x}Ge_x$ barrier must be tensile strained (x>y) to compensate the compressive stress in the QW. The average silicon concentration in the Ge/SiGe MQW region is designed to be the same or similar to that in the buffer. The strain forces of the compressed Ge and extended SiGe layers of each QW pair cancel out, and no strain energy accumulates into the next pair. Theoretically this would enable

extension of the strained layer thickness beyond the critical thickness limitation to infinity.

Since all quantum-well layers are strained relative to the buffer, their $a_{\parallel}$ are the same, but the $a_{\perp}$ of the Ge well (and the SiGe barrier) is larger (and smaller) than its original value due to the strain. This property can be used to examine the balance of deposited quantum wells by XRD.

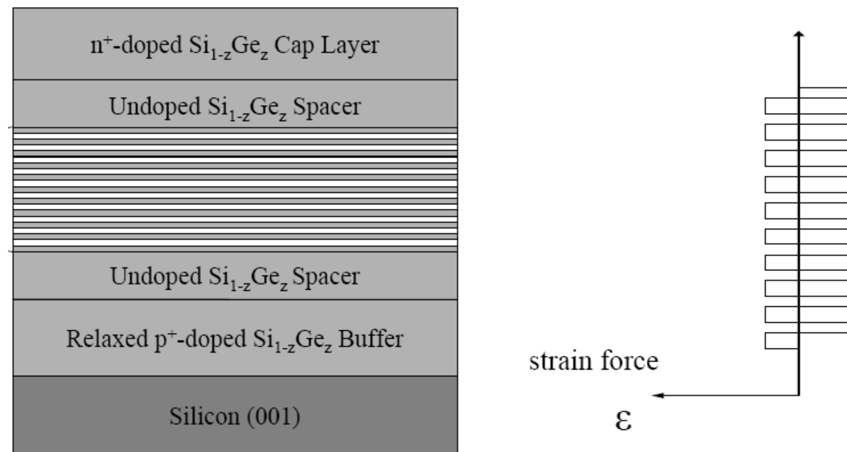

Figure 4.18: Strained Ge/$Si_{1-x}Ge_x$ quantum well structure on relaxed $Si_{1-z}Ge_z$ buffer and its strain balance.

4.7.2 Growth of Multiple-Quantum-Well Structures

After the growth and annealing of Ge-rich SiGe buffers, Ge/SiGe MQWs were deposited at the same 400 ºC growth temperature. The growth rates of Ge wells and SiGe barriers were kept at ~10 nm/min. Before the growth of each well and barrier layer, the gas lines of Si and Ge sources were switched into the "Vent" mode for 20~40 s with only H_2 carrier gas flowing into the chamber. This step provides enough time to adjust the silane and germane flux rates for the next deposition as well as to purge the chamber to make the MQW interfaces sharp.

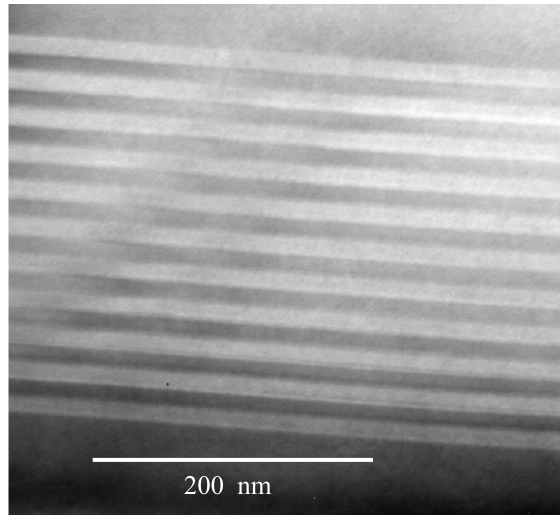

Figure 4.19: Cross-sectional TEM image of 10-pair MQWs grown on SiGe on Si.

Fig. 4.19 is a cross-sectional TEM image of 10 pairs of strained Ge/SiGe QWs grown on relaxed SiGe on Si. The Ge well is 10 nm and the $Si_{0.15}Ge_{0.85}$ barrier is 16 nm. The sharp and regular MQW structure provides steep barriers for better carrier confinement and improves the optical quality.

Since there is a 4% lattice mismatch between Si and Ge, the SiGe heterostructure is highly strained. The key thing is to check if the Ge/SiGe MQW region is strained and if the Ge-rich SiGe buffer region is fully relaxed. XRD was used to examine the strain balance in the grown structure. Fig. 4.20 shows the comparison between the XRD measurement and theoretical simulation. The x-axis of the plot is the diffraction angle which corresponds to the vertical lattice spacing (when the sample surface is normal to the common plane of the incident and diffracted beams), and the y-axis is the X-ray count rate. The sample consists of 10 pairs of Ge/SiGe QWs (10 nm Ge well/16 nm $Si_{0.15}Ge_{0.85}$ barrier) on a relaxed $Si_{0.1}Ge_{0.9}$ buffer on silicon. The simulation was done with Philips X'Pert Epitaxy. First, the measured peak of the relaxed SiGe buffer resides on the simulated position, thus the Ge-rich buffer is fully relaxed. Secondly, the buffer peak is obviously surrounded by several other peaks from the

Ge/SiGe MQWs, which indicates a high MQW quality in this sample since it is difficult to observe that in SiGe/Si MQWs even when they are in the Si-rich end. Finally, the peaks of the Ge/SiGe MQWs from the measurement and simulation also agree well – this proves the MQW structure is strained relative to the relaxed SiGe buffer.

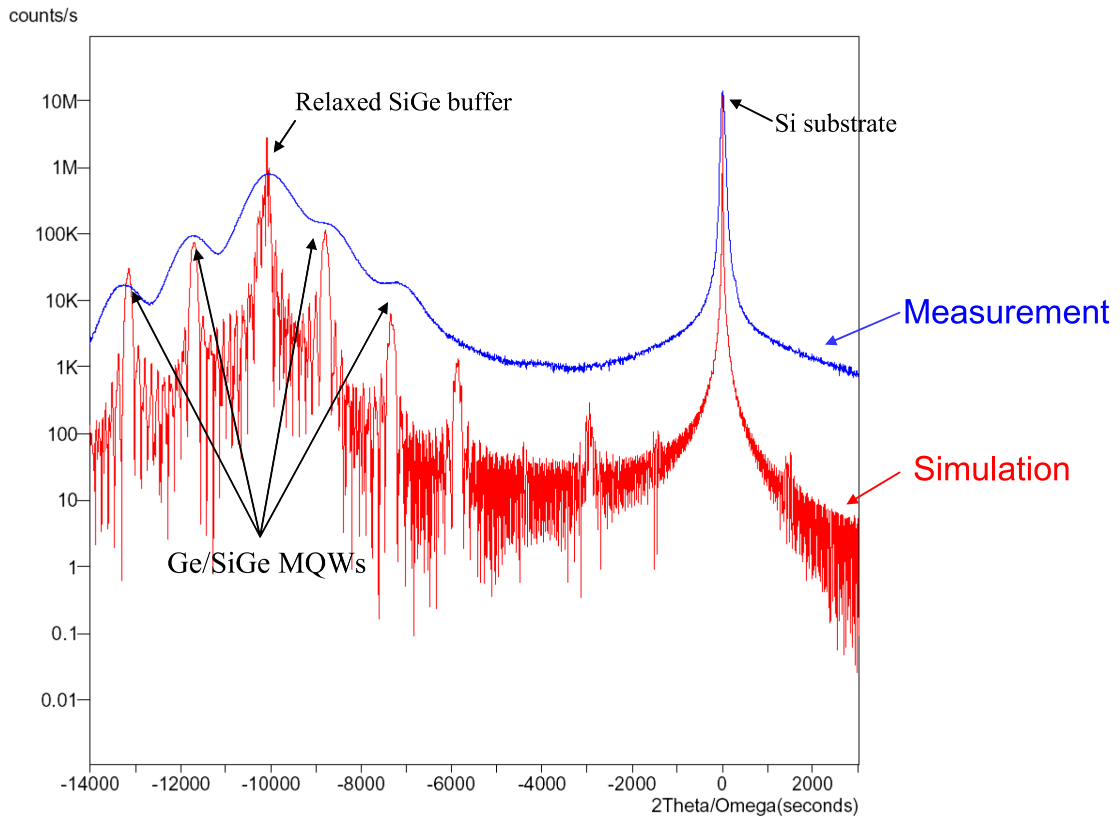

Figure 4.20: Comparison between XRD measurement (blue line) and theoretical simulation (red line).

Chapter 5 Device Fabrication and Characterization

5.1 Device Fabrication

Our germanium-silicon modulator devices are SiGe p-i-n diodes on Si with Ge/SiGe quantum wells in the i-region. The Ge/SiGe quantum-well structures were grown by RPCVD. The deposition of Ge-rich SiGe or pure Ge films on Si substrates usually requires thick graded buffer layers to reduce the threading dislocation density, but here we used thin, direct deposition of SiGe buffers on Si described in Chapter 4, instead of the thick graded buffer method. In order to control the SiGe composition in the buffer and the strain in the Ge/SiGe MQWs, a single growth temperature of 400°C was used for all layers.

Fig. 5.1 shows the device fabrication processes. 4-inch, (001)-oriented, boron-doped Si wafers with resistivity 10-20 Ω-cm were used as starting substrates. Two boron-doped Ge-rich SiGe layers (p-type dopants with doping levels ~$5x10^{18}$ cm^{-3}) were deposited on silicon sequentially and annealed. The first 250nm layer was annealed at 850 °C for 30-60 min, and then a second 250 nm SiGe layer was deposited at 400 °C and annealed at 700 °C for 5 min. Undoped Ge/SiGe quantum wells with

spacers were then deposited and capped by arsenic-doped layers (n-type dopants with doping levels ~ 1×10^{19} cm^{-3}).

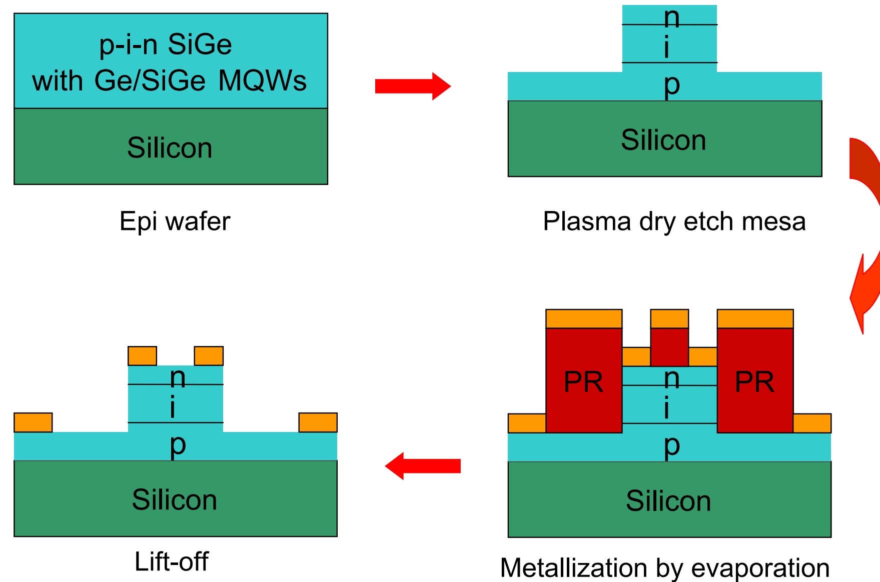

Figure 5.1: Device process flow.

To form square mesa structures, epi wafers were coated with 1μm thick photoresist (Shipley 3612) in the SVG coater, using the standard recipe with edge bead removal. It was then patterned, using optical lithography in the Karl Suss MA-6 aligner and developed in the SVG developer. The mesas were plasma dry etched to reach the bottom p-doped region with CF_4 etchant in the Drytek2 etcher.

Rectangular ring contact regions were patterned with 1.6μm thick photoresist (Shipley 3612), again using the SVG coater, Karl Suss aligner, and SVG developer. Metal layers, including 15-30 nm Ti and 300-1000 nm Al, were deposited by electron beam evaporator. The metal was lifted-off in acetone/methanol/isopropanol solvents and then annealed at ~350-400 ºC for ~1-3 min in the rapid thermal annealer (RTA) to form ohmic n- and p- contacts.

For high-speed measurements or surface passivation purposes, an optional insulation layer can be used (though the devices measured in this chapter were not protected with an insulator). The steps of the insulator deposition, patterning, and etching would be inserted after the mesa etching and before the metal evaporation. The insulation material can be oxide, nitride, or both of them to balance their thermal expansion mismatch. The insulator was deposited in the STS low-temperature plasma-enhanced CVD (RPCVD) at 350 ºC. This layer can isolate the side-walls of mesa diodes from air, terminate the surface dangling bonds, and reduce the surface leakage current. It is also necessary for high-speed devices as an isolation layer between the metal pads and silicon substrate. A high-speed device layout with the insulator layer and ground-signal-ground (GSG) pads is shown in Fig. 5.2(a), and a fabricated Ge-Si modulator device based on the layout is shown in Fig. 5.2(b). This kind of device will be used for future high-speed measurements.

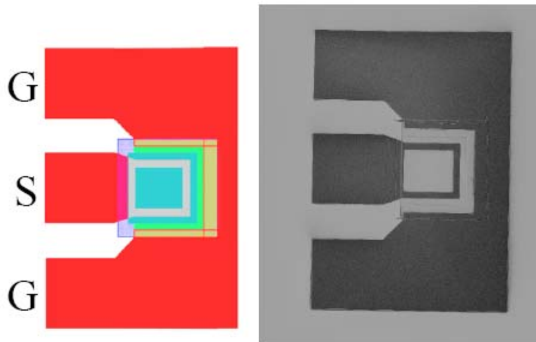

Figure 5.2: (a) 4-mask-level GSG layout for high-speed Ge/SiGe devices. (b) SEM image of a fabricated 100x100 μm Ge/SiGe modulator device.

All materials used here, including silicon substrates, SiGe epi-layers, and Ti/Al contact metal, are also used in standard silicon chip fabrication. The growth and processing equipment are standard CMOS fabrication tools. The process temperatures, except the annealing steps, are at 400 ºC or less, which are even compatible with the CMOS back-end thermal budget.

5.2 Absorption Measurement

Both photocurrent and transmission measurements can be used to measure the absorption coefficient and its electric-field dependence; however, the former is a better method in order to obtain detailed information in the low absorption coefficient region. Here the absorption spectra are extracted from photocurrent measurements with different bias voltages. Fig. 5.3 shows the absorption measurement setup.

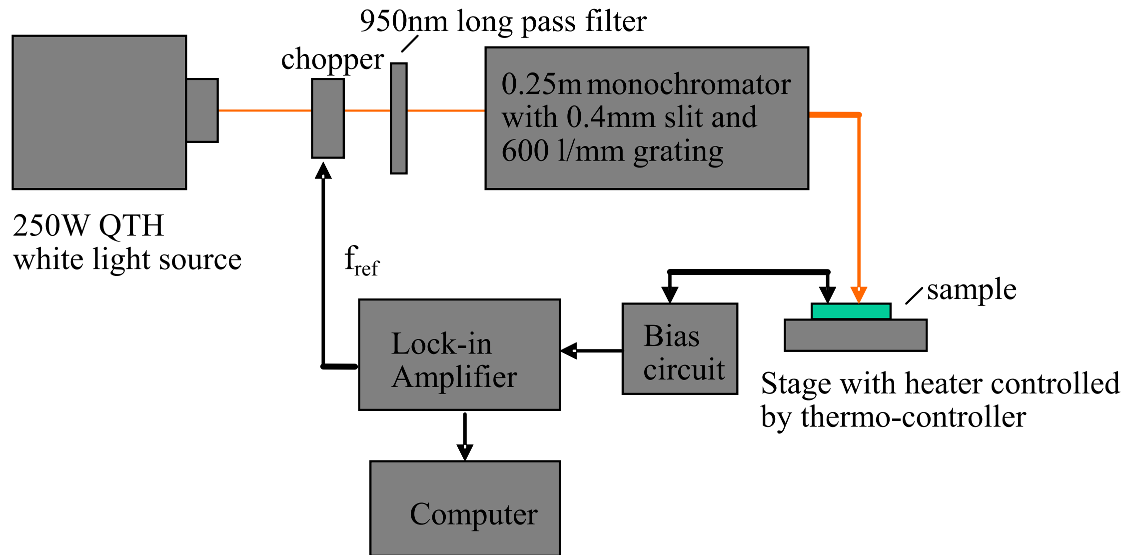

Figure 5.3: Absorption measurement set-up.

Though the device chip could be directly probed, for convenience the chip was epoxied into a 24-pin ceramic side-brazed dual-in-line package (DIP) from Spectrum Semiconductor (CSB02442), as shown in Fig 5.4. The packaged chip was mounted on a modified, temperature-controlled cryostat (Cryo Industries CSM-1161-C) on an X-Y-Z stage. The cryostat temperature was controlled by a Conduct LTC-10 temperature

controller, and the real chip temperature was measured by a thermocouple temperature sensor.

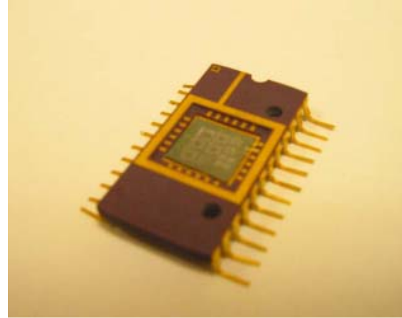

Figure 5.4: A packaged Ge-Si modulator chip.

The light source was a 250 W quartz-tungsten-halogen (QTH) white-light bulb in an Oriel Research Housing (model 66181) and powered by an Oriel 68830 constant current supply. This kind of light source can provide a broad spectrum and is more suitable for wide range absorption measurements. The light first passed through a long-pass filter with a 950 nm cut-off wavelength, and was then chopped at a frequency of 317 Hz set by a Stanford Research Systems (SRS) chopper controller (SR540), and finally passed through a 0.25 m monochromator (Oriel 77200) with a 0.4 mm slit and a 600 l/mm grating. This gave single-wavelength light with a full-width-half-maximum (FWHM) line-width ~2.7 nm.

The light power spectrum was measured with a Newport 818-IG InGaAs photodetector as a reference for responsivity calculations. During the absorption measurement, the light was normally incident into the device with random polarization. The p-i-n device was reversely biased by a biasing circuit. The photocurrent was then measured and extracted by a lock-in amplifier (SRS SR830). Assuming one electron of current for each absorbed photon, the responsivity was obtained by dividing the photocurrent from the light power passing through the i-region. The surface reflections were corrected and the corresponding effective absorption coefficient was calculated based on the total MQW region thickness (including well and barrier thicknesses).

5.3 The First Strong QCSE in Group-IV Material Systems

The very first QCSE in Ge/SiGe quantum wells and also in group-IV material systems was observed in the device design shown in Fig. 5.5. It has a 500 nm relaxed boron-doped $Si_{0.1}Ge_{0.9}$ p-type buffer grown on silicon, an intrinsic region containing 10 pairs of strained quantum wells (including 10 nm Ge well and 16 nm $Si_{0.15}Ge_{0.85}$ barrier) and two 100 nm $Si_{0.1}Ge_{0.9}$ spacers, and a 200 nm arsenic-doped $Si_{0.1}Ge_{0.9}$ n-type cap layer.

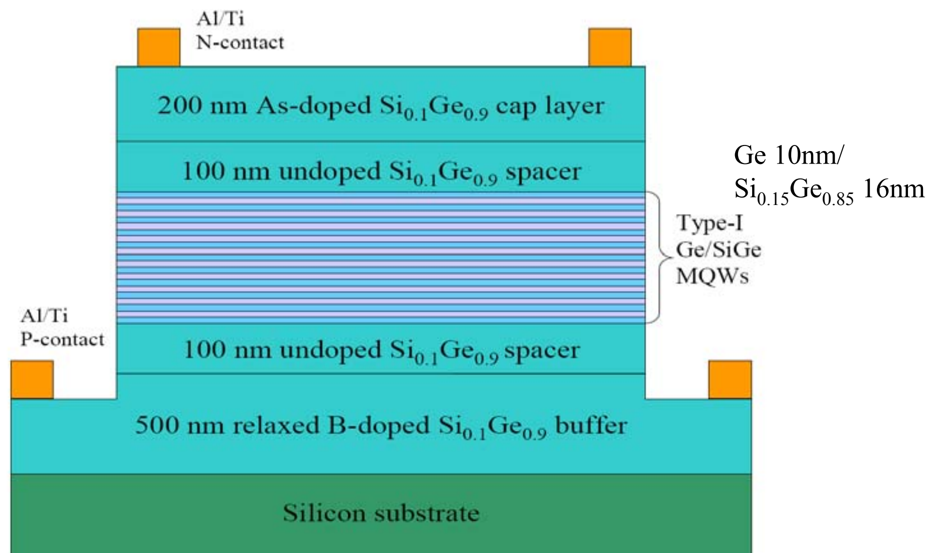

Figure 5.5: Cross-sectional schematic of a p-i-n device with Ge/SiGe MQWs in the i-region.

The effective absorption coefficient spectra measured at room temperature for this device are shown in Fig. 5.6. The thickness for the effective absorption coefficient calculation is based on the total thickness (~0.26 μm) of 10 pairs of Ge wells and SiGe barriers. The exciton peaks related to the electron-heavy-hole (e-hh) transition and electron-light-hole (e-lh) transition are obvious. The observation of clear exciton peaks at room temperature (compared to that of bulk Ge [91]) is the result of carrier

confinement in the quantum wells (see Sec. 2.2). The band-edge effective absorption coefficient is also enhanced by the quantum confinement to 6320 cm^{-1}. The initial absorption edge is shifted to 0.88 eV from the direct band gap energy, 0.8 eV, of bulk Ge by both the quantum well energy and strain effect.

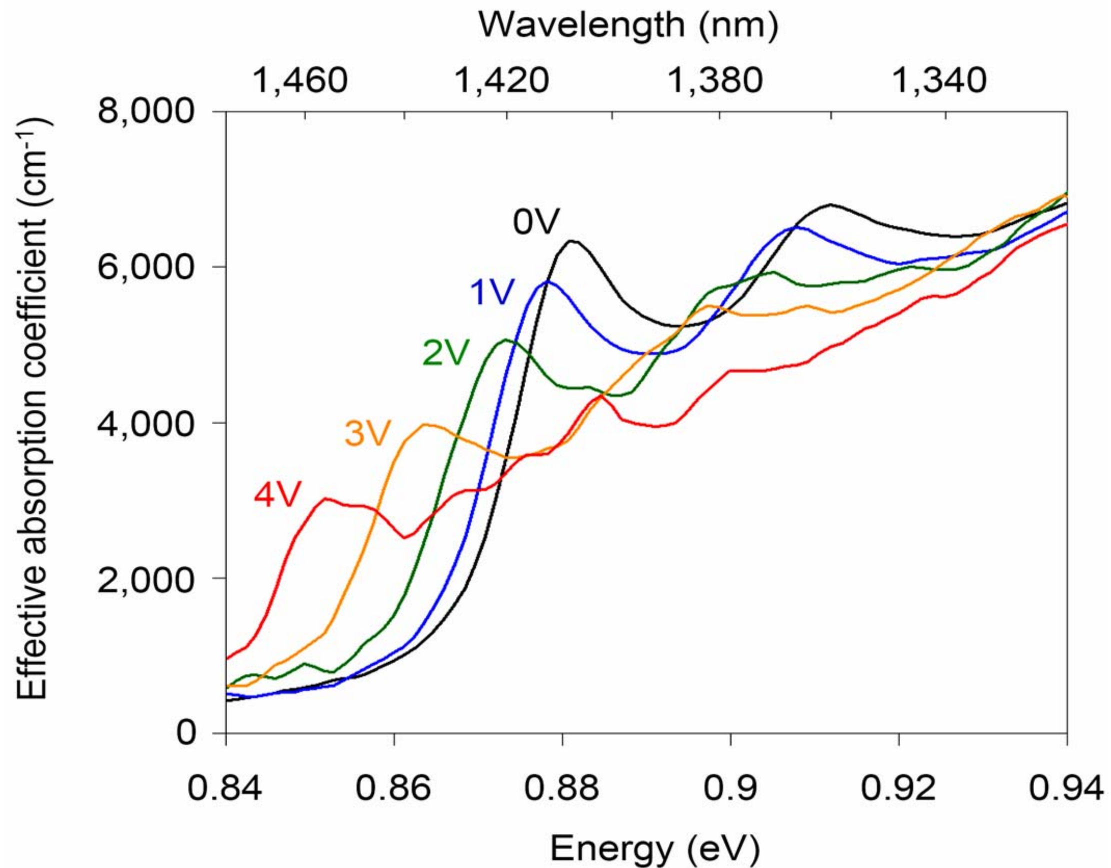

Figure 5.6: Effective absorption spectra of the p-i-n device with 10 nm Ge quantum well structure measured at room temperature with reverse bias from 0 to 4 V. The thickness for the effective absorption coefficient calculations is based on the combination of Ge well and SiGe barrier thicknesses.

Since the Ge wells are under compressive strain, the heavy hole band becomes the topmost valence band and the band-edge absorption peak is related to the heavy-hole exciton. It has only 16 meV full resonance width at zero bias and is still easily resolvable under 3V reverse bias. Also, the effective absorption coefficient at high

energies (far from the band-edge) under 0 V bias is similar to that under high reverse bias voltages. The high responsivity without any bias voltage indicates that the i-region of this p-i-n device is highly intrinsic with a low background doping level, and hence the built-in field depletes the whole i-region and sweeps all photo-generated carriers to be collected. This is also advantageous for these electroabsorption modulators to be used as photodetectors.

With the reverse bias increased from 0 V to 4 V, the absorption edge is Stark shifted from 1408 nm to 1456 nm. The maximum change of the effective absorption coefficient is 2800 cm^{-1} at 1438 nm under 3 V bias. Fig. 5.7 shows the spectra of the effective absorption coefficient ratio between the biased and non-biased conditions. For the case of 4 V to 0 V bias voltage, the peak contrast ratio is 4.69 at 1461 nm, and the contrast is larger than 3 over a bandwidth ranging from 1443 to 1471 nm.

The behavior of the exciton peaks in this Ge quantum well system is similar to that in type-I direct band gap systems, and the magnitude is also comparable to or even stronger than that of III-V compounds at similar wavelengths [92].

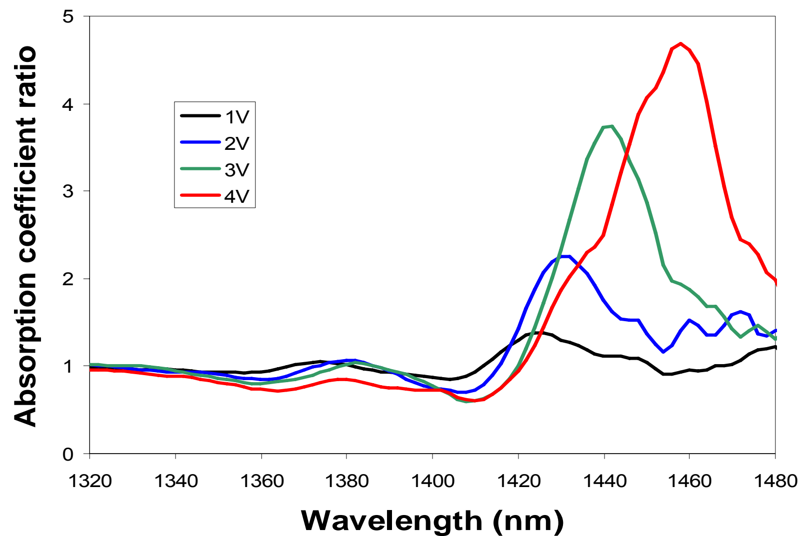

Figure 5.7: Spectra of absorption coefficient ratio between bias and non-bias conditions.

5.4 Devices for C-Band Operation

The Strong electroabsorption effect has been observed in the 10 nm QW device; however, the initial absorption edge is shifted from 1550 nm to a shorter wavelength by the strain effect and quantum confinement energy such that the operation wavelength resides around 1440-1470 nm. Though the operation wavelength here might not be an issue for short-distance optical interconnections, it is still desirable to have C-band operation (~1530-1565 nm) for compatibility with long-haul optical communications. Besides, it is inevitable that such devices will operate in a higher-temperature environment when integrated with CMOS chips, so the high temperature should also be considered.

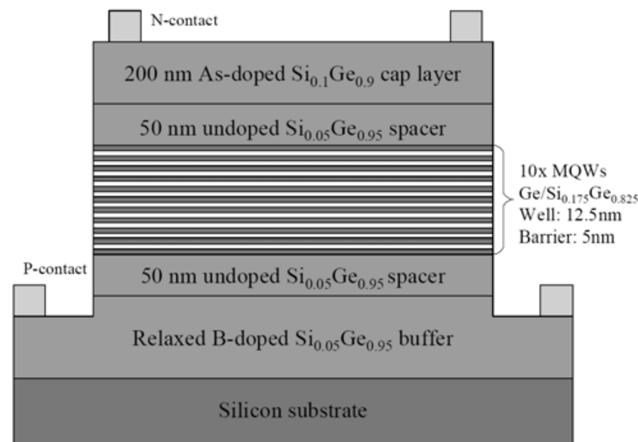

Figure 5.8: Cross-sectional schematic of a p-i-n device with Ge MQWs for C-band operation.

Taking all these factors into consideration, as well as the ~100 nm wavelength difference between C-band and the operating wavelength (~1460 nm) of the 10 nm QW device, a new structure was designed to increase its operating wavelength (i.e. to reduce the transition energy) by: (i) high operating temperature: the ~ 60 ºC difference between room temperature and the CMOS chip operating temperature would reduce the band gap energy and push the wavelength back by ~50 nm; (ii) quantum well

energy: the quantum well thickness was increased from 10 nm to 12.5 nm to reduce the confinement energy, especially in the conduction band; (iii) strain energy: the silicon concentration was reduced from 10% to 5%, thus the strain between the Ge well and relaxed SiGe buffer decreases to half.

Moreover, the thicknesses of barriers and spacers were also reduced to decrease the operating voltage. The new design is shown in Fig. 5.8. It has a relaxed, boron-doped $Si_{0.05}Ge_{0.95}$ p-type buffer, an intrinsic region contains 10 pairs of strained quantum wells (including 12.5 nm Ge well and 5 nm $Si_{0.175}Ge_{0.825}$ barrier) and two 50 nm $Si_{0.05}Ge_{0.95}$ spacers, and a 200 nm arsenic-doped $Si_{0.05}Ge_{0.95}$ n-type cap layer.

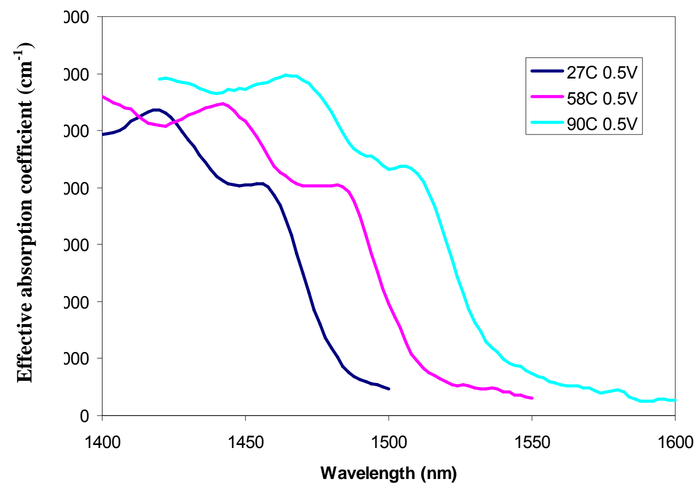

Figure 5.9: Effective absorption coefficient spectra of the p-i-n device with 12.5 nm Ge quantum well structure under 0.5V reverse bias at different temperatures.

Fig. 5.9 shows the effective absorption coefficient spectra under 0.5 V reverse bias at different temperatures for the 12.5 nm QW device. The thickness for the effective absorption coefficient calculation is based on the total thickness (~0.175 μm) of 10 pairs of Ge wells and SiGe barriers. When the device is heated up from room temperature to 90 °C, the absorption curves show a monotonic shift in wavelength without much magnitude change. The exciton peak is still resolvable at high

temperatures and moves from 1456 nm to 1508 nm, corresponding to a temperature dependence of band gap energy ~0.83 nm/°C (~0.47 meV/°C).

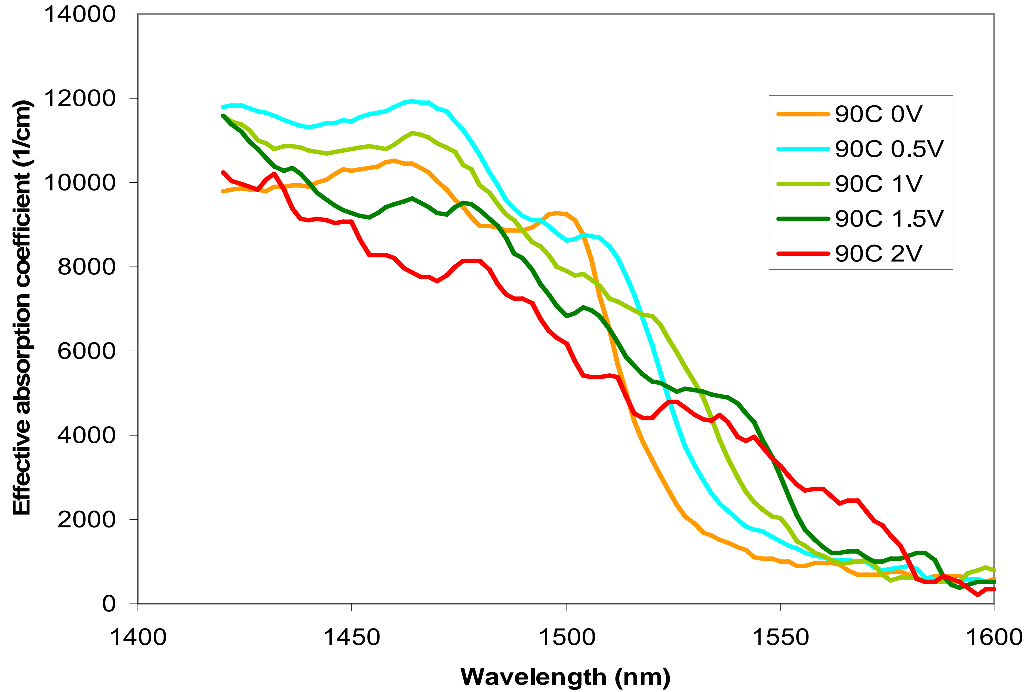

Figure 5.10: Effective absorption coefficient spectra of the p-i-n device with 12.5 nm Ge quantum well structure measured at 90 ºC with reverse bias from 0 to 2 V.

Fig. 5.10 shows the effective absorption coefficient spectra under different reverse bias voltages at 90°C operation. The effective absorption coefficient of the exciton peak under zero bias is 9240 cm^{-1}. With 0 V to 2 V reverse bias at 90°C, the absorption edge shifts from 1500 nm to 1560 nm by the QCSE. The effective absorption coefficient has a maximum change of 2703 cm^{-1} at 1538 nm between 0 V and 1.5 V bias. The peak contrast of effective absorption coefficients between 0 V and 2 V bias is 3.6 at 1564 nm, and the optical bandwidth with absorption coefficient contrast higher than 3 is 20 nm.

Though the increased quantum well thickness has reduced the confinement and weakened the exciton binding, the magnitude and shift of the QCSE are still

comparable to those of III-V materials at similar wavelengths. These results prove the QCSE in the germanium quantum well system is robust and still observable, even at high operating temperatures. Ge-Si electroabsorption modulators can operate in the high temperature environments of CMOS chips and cover the whole 1530-1560nm C-band wavelength region.

5.5 Discussions

5.5.1 Comparisons between Experimental and Theoretical Results

Both devices in the previous sections have strong QCSE and large Stark shifts, mainly from the heavy-hole exciton shifts. These Stark shifts from experimental measurements (square dots) are compared with theoretical simulations (solid) in Fig. 5.11(a) for the 10nm QW device and in Fig. 5.11(b) for the 12.5 nm QW device. The theoretical simulations are calculated by the resonance tunneling method and based on the assumption of full confinement at the Γ point in the conduction band (See Sec. 3.3). Both results agree very well, though slightly larger Stark shifts are observed experimentally in both samples, especially under high electric fields.

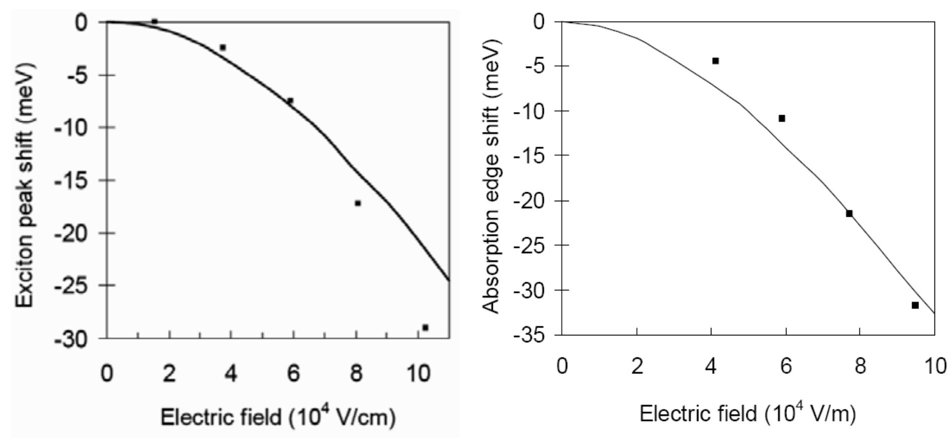

Figure 5.11: Comparisons of Stark shifts from experimental results and resonance tunneling simulations in (a) 10 nm (b) 12.5 nm quantum well samples. Both cases show good agreements.

The initial heavy-hole exciton peaks of the 10 nm and 12.5 nm QW devices measured at room temperature are shifted from their bulk absorption edge by compressive strain (the Ge well strained to the relaxed SiGe buffer) and quantum well energy. The calculated increment caused by strain [58] is 36 meV (and 19 meV), and the simulated quantum well energy under 0 V bias (see Sec. 3.3) is 56 meV (and 39 meV) for the 10 nm (and 12.5nm) QW sample. The combinations of these calculated increments basically agree well with the experimental results, though the theoretical one is 12 meV (and 8 meV) higher than the experimental one for the 10 nm (and 12.5 nm) device. The discrepancy might result from neglecting the exciton binding energy correction (which reduces the increment) as well as the uncertainty in the band parameters and electron effective mass at the Γ point.

5.5.2 QCSE and the Confinement in the Direct Conduction Band

From the comparisons between the experimental results and theoretical simulations, it is clear that the exciton shifts, the initial band-edge energy increments, and the clarity of excitons all agree well with the assumption that electrons at the zone center are confined in the wells by the direct conduction band discontinuity and would not tunnel into the barrier rapidly, even though the conduction band minimum at the Γ point is higher than the global minima. In this case, the global minima are in the L valleys (the [111] orientation) (it can also be the Δ valleys (the [100] orientation) if higher Si contents in the buffers and barriers are used in different designs) (See Sec. 2.2), so the tunneling (or coupling) of electrons from the Γ point into the L or Δ valleys is difficult due to the different momentum orientations in the k-E diagram. Besides, the periodic part of the Block wave function at the Γ point is center-symmetric to the zone center (S-like), while that of the L or Δ valleys is 8-fold or 6-fold symmetric, so their overlap weakens the coupling of the electrons between the Γ point and side valleys.

Moreover, the lowest-energy (ground-state) electrons at the Γ point have near zero momentum perpendicular to the quantum well growth direction and only have a little momentum parallel to the growth direction (due to quantum confinement; e.g., the thicknesses of our wells are thicker than 10nm, i.e. 20 times that of the Ge lattice constant a_o, so k is [$\pi/20a_o$, 0, 0]). It is impossible for electrons in the indirect Δ or L valleys to have the same energy (~0.8 eV) and momentum at the same time (see the Ge band diagram), and hence it requires at least several electrons for coupling or phonon-assistance for scattering.

It is not necessary to have an extremely high barrier height to confine electrons inside the quantum well. In the case of GaAs/AlGaAs QW [93], only several percent of Al in the barrier can provide enough confinement for electrons to exhibit the QCSE. Since the conduction band discontinuity at the Γ point in our case is more than 0.4 eV, it is sufficiently high to confine electrons in the quantum wells and bind them with holes to form excitons.

It is also interesting that the QCSE in the Ge/SiGe system is comparable to or even stronger than that in III-V compounds at similar wavelengths [92] or in indirect III-V QW systems [94, 95]. The key reasons are that the well here is pure Ge with no alloy effect (a random distribution of elements broadens the exciton peaks and absorption edge) and also the interfaces between the quantum wells and barriers in the RPCVD-grown samples are sharp (maybe enhanced by hydrogen in the reactor). Though the scattering time of electrons from the direct conduction band into the indirect band in bulk Ge is about 0.5 ps [96], the absorption time and the exciton ionization time are less than that [97, 98], and hence the scattering of electrons into the side valleys in the same well (or in the barriers) does not broaden the exciton peaks appreciably. However, the exciton peaks here are still slightly broader compared to those of MBE-grown GaAs/AlGaAs quantum wells whose GaAs layers also have no alloy problem.

We also notice that though the measured initial peak positions and their Stark shifts basically agree well with the theoretical simulations, the initial peaks are relatively lower than the theoretical expectations and the Stark shifts are slightly stronger than the simulated ones. These differences might be caused by the neglected exciton effects or the uncertainty in the strain effects, but they also might come from non-full quantum confinement in the conduction band (which is actually not really undesired here because the high initial quantum well energy in our case pushes the operating band edge out of C-band). This provides a tantalizing opportunity that a structure with partial quantum confinement and a relatively lower quantum well energy (for C-band operation) in the conduction band can still exhibit strong or moderate QCSE because (i) the Stark shift is dominated by holes and (ii) the absorption in the barrier is prohibited or not efficient (the direct band gap energy in the barrier is far higher and hence any electron tunneling from the well into the barrier becomes indirect and cannot be involved in the absorption process as efficiently as those electrons in the well). The drawback of non-full confinement is that the exciton effect would be relatively weak. However, the indirect conduction band offset is small, and hence full electron confinement only pushes the direct band edge into a shorter wavelength region with higher indirect gap (background) absorption. If we can shift the direct transition energy back to the original point, the background absorption will be reduced, which compensates for the weaker exciton effect. The other way to achieve strong or moderate QCSE without strong electron confinement and high quantum well energy in the conduction band is to increase the quantum well thickness, such as the 12.5 nm QW device.

5.5.3 Speed

Theoretically quantum-well modulators can operate into the THz regime [99] because of fast excitonic transitions; however, the speed in practical applications is limited by

the intrinsic carrier transport and extrinsic electrical parasitics (*RC*-limited). The photo-generated electrons and holes in the i-region transfer into the n-region and p-region respectively through tunneling, thermionic emission, or drift processes. The high conduction band barrier in III-V quantum well devices slows the first two transfer processes for electrons and reduces the operation speed. Further, carrier accumulation in quantum wells causes optical nonlinearities by saturation effects, such as phase-space filling and plasma-induced Coulombic field screening [100, 101]. In Ge/SiGe quantum well structures, these kinds of problems might not exist because the electrons can be easily swept out of the Γ point into the side valleys where the conduction band confinement is very shallow. Moreover, the hole mobility in Ge (~2000 cm^2/Vs) is the highest value among major semiconductors and largely enhances the drift speed. These features make Ge modulators promising for high-speed applications. For the p-i-n device shown in Fig. 5.5 with 100 μm^2 surface area, e.g., the capacitance is 30fF and the resistance is ~20-150 Ω (depending on the device aspect ratio and contact geometry), so the operation speed is expected to reach tens GHz in a square device and over hundred GHz in a waveguide structure.

5.6 Summary

SiGe p-i-n devices with strained Ge/SiGe quantum wells in the i-region were grown on relaxed SiGe buffers on Si substrates. The processes were totally based on CMOS fabrication tools. Strong quantum-confined Stark effect has been observed in these group-IV quantum devices. The effect here is comparable to that in III-V material systems at similar wavelengths. The experimental results agree well with tunneling resonance simulations. The operation of the specially designed device for the high temperature environment in silicon chips can also cover the whole C-band wavelength range for telecommunication compatibility. This will enable efficient Ge modulators on silicon for optical interconnects with silicon electronics.

Chapter 6 Analysis of Modulator Configurations

The electroabsorption effect is the most efficient optical modulation mechanism with a large value of absorption coefficient change - it can change the light intensity significantly in a short distance. Since light passing through the quantum well region from varying angles can be modulated, both vertical and lateral modulator configurations are possible. In this chapter the two most commonly practiced modulator configurations, vertical asymmetric Fabry-Perot modulators (AFPMs) and lateral waveguide modulators, will be discussed and compared.

6.1 Vertical Modulators

For vertical modulators, the light passes through the QW region vertically and is modulated by the change of the absorption coefficient (such as AFPMs and vertical transmission modulators) or refractive index (such as phase-flip and direction-flip modulators) (See, e.g., ref. [102]). The former has higher efficiency than the latter; however, the thickness of the QW region is typically in the order of 1 μm or less, so the modulation is not significant unless using a resonator structure. With a resonant cavity, the contrast or extinction ratio can be enhanced at the expense of optical bandwidth. The commonly used AFPM structure is shown in Fig. 6.1, which can give

very high contrast ratio. Ideally the back mirror reflectivity is 100%, and the front mirror reflectivity depends on the quantum well design and does not necessarily have to be high. In the III-V compound system, distributed Bragg reflectors (DBRs) are commonly used as the front and back mirrors. DBR mirrors are also developed in the Si/SiGe system [103, 104] (though not as perfect as III-V ones) and suitable for the front mirrors. Metal-coated surfaces or oxide/nitride stacks are also useful for mirrors.

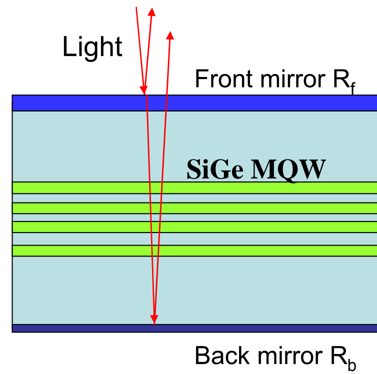

Figure 6.1: Schematic of asymmetric Fabry-Perot modulator.

During operation, light is shined into the modulator from a fiber or free space. Part of the light is reflected by the front mirror, and the other part passes through the front mirror into the cavity. The light inside the cavity is partially absorbed by the quantum wells and reflected by both the back and front mirrors. This process iterates multiple times until the light passes through the front mirror again, thus the modulation effect is significant. The two beams interfere with each other and cause intensity modulation of the total reflection. The light inside the cavity can be treated as two opposite traveling EM waves with the boundary conditions based on the front and back mirrors [105]. For a vertical cavity reflection modulator, the total reflectivity under Fabry-Perot resonance condition (when the cavity length is a half integer multiple of the wavelength) can be expressed as [106]

$$R_{tot} = (\frac{r_f - r_{beff}}{1 - r_f r_{eff}})^2 \tag{6.1}$$

where r_f is the front mirror reflection coefficient and r_{beff} is the effective back mirror reflection coefficient including the effects from the real back mirror reflection and the single-path absorption loss through the QW region.

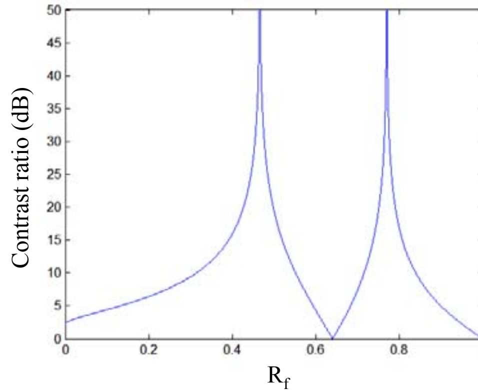

Figure 6.2: Contrast ratio simulated as a function of the front mirror reflectivity at Fabry-Perot resonances. The ratio is only shown to 50dB in the plot and can actually reach infinity under matching conditions. A wide-range of the front mirror reflectivity can achieve high contrast ratio.

When the absorption coefficient in MQWs is changed by the bias voltage, the total reflectivity is modulated. Assuming that metal is used as the back mirror with a reflectivity R_b of 95% as well as the single path loss through MQWs is changed from 10% to 30% (a moderate 3:1 ratio), the contrast ratio, $R_{tot(\text{on-state})}/R_{tot(\text{off-state})}$, under Fabry-Perot resonance condition is simulated as a function of the front mirror reflectivity R_f and shown in Fig. 6.2. When the absorption loss is increased, the reflectivity actually can drop or increase, so the on-state may correspond to a low or high absorption condition, and hence two peaks are found. A high contrast can be achieved in this configuration, but the drawback is the narrow optical bandwidth due to the resonance limitation. There are several ways to enhance the optical bandwidth, including the reduction of the cavity length, the reduction of the front mirror reflectivity, and the use of the tilt-angle incidence instead of the vertical incidence (such as QWAFM [92]).

6.2 Lateral Waveguide Modulators

In order to utilize the full optical bandwidth of a material system, the use of resonator structures should be avoided. A lateral waveguide modulator is a more appropriate configuration because it can provide a longer optical interaction length without any resonator cavity in the direction of light propagation. Besides, its length is much longer than the thickness of the vertical cavity, so it requires fewer quantum well layers and is suitable for low voltage operation. If there is background absorption present in the absorption spectrum, the waveguide will absorb light even without bias. The insertion loss is proportional to the effective active waveguide length, and so is the contrast ratio.

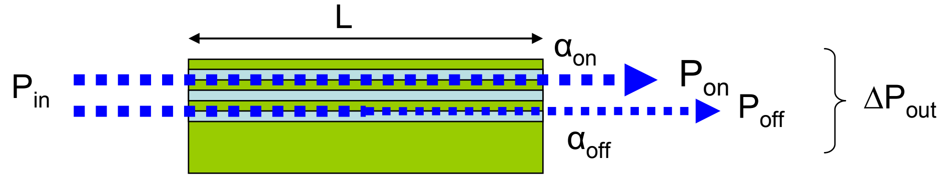

Figure 6.3: Schematic of lateral configuration. The light passing through quantum well structure is modulated into the on-state or off-state, depending on the voltage-tunable absorption coefficient α.

Fig. 6.3 shows the schematic of a lateral modulator with a QW region whose effective absorption coefficient depends on the applied bias voltage. The effective length L_{eff} is defined as the product of the length (L) in the active waveguide region times the confinement factor (Γ, which weights the overlap of the MQWs region and the optical power of the propagating light). The input light intensity is P_{in}, and the absorption coefficients are α_{on} and α_{off} ($\alpha_{on} < \alpha_{off}$) for the on-state and off-state respectively. The light output intensities are

$$P_{out(on-state)} = P_{in} \cdot e^{-\alpha_{on} \cdot L_{eff}} \qquad (6.2)$$

$$\& \; P_{out(off-state)} = P_{in} \cdot e^{-\alpha_{off} \cdot L_{eff}} \qquad (6.3)$$

for the on-state and off-state respectively ($P_{out(on\text{-}state)} > P_{out(off\text{-}state)}$) after being absorbed under different bias conditions. The insertion loss (*IL*) and contrast ratio (*CR*) are

$$IL = \frac{P_{in}}{P_{out(on-state)}} = e^{\alpha_{on} \cdot L_{eff}} \tag{6.4}$$

$$\& \ CR = \frac{P_{out(on-state)}}{P_{out(off-state)}} = e^{(\alpha_{off} - \alpha_{on}) \cdot L_{eff}} \tag{6.5}$$

respectively. However, instead of merely optimizing the insertion loss or contrast ratio, we would like to maximize the real signal which is the output power difference

$$\Delta P_{out} = P_{out(on-state)} - P_{out(off-state)} . \tag{6.6}$$

Define $r = \alpha_{off}/\alpha_{on}$ as the ratio between the off-state and on-state absorption coefficients. Under the maxima-power-difference scheme, the insertion loss, contrast ratio, and output power level depend only on *r*, and it is also interesting that the contrast ratio CR is the same as the absorption coefficient ratio *r*.

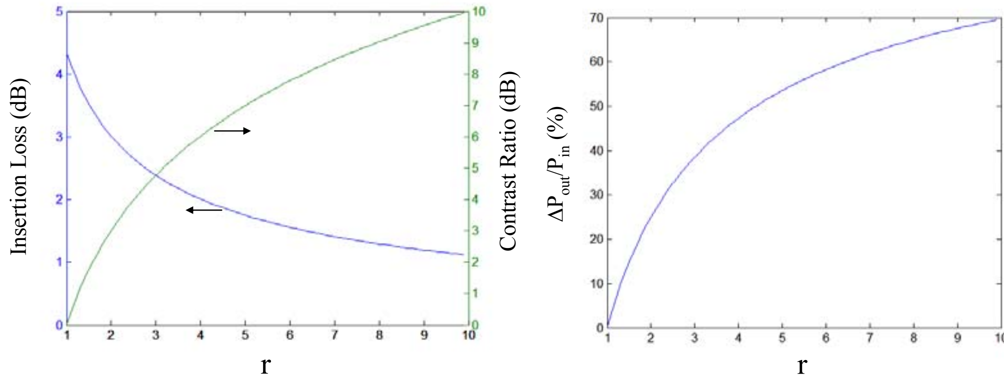

Figure 6.4: (a) Insertion loss, contrast ratio, and (b) optical power difference for different ratio r in the maxima-power-difference scheme simulation.

Fig. 6.4(a) plots the insertion loss and contrast ratio as a function of the absorption coefficient ratio *r*. For a moderate 3~5 absorption coefficient ratio, it can give a

contrast ratio ~6dB and insertion loss ~2dB. Fig. 6.4(b) shows ΔPout/Pin as a function of *r*. When *r* is 3~5, the power efficiency in this modulator configuration is ~40%. This is a very efficient modulator design with a short device length and high optical bandwidth. Besides, a higher *r* would not improve the signal level significantly. Now the key to increase the total system performance is by reducing the noise level in the receiver-end, especially for Ge-based photodetectors, because the transmission system capacity is determined by the bandwidth and signal-to-noise ratio (SNR) based on the Shannon capacity theorem [107].

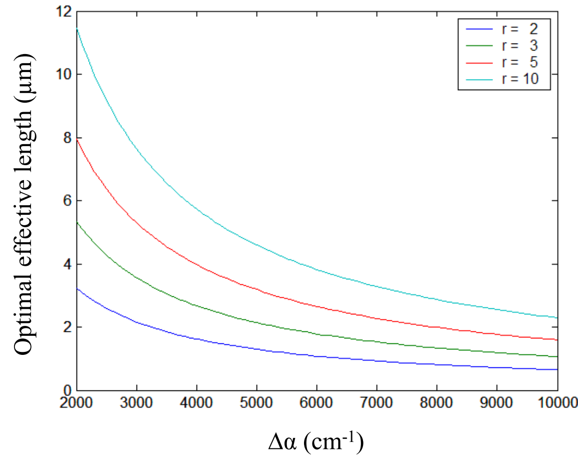

Figure 6.5: Dependence of optimal effective length on absorption coefficient changes Δα with various *r* in the maxima-power-difference scheme simulation.

Fig. 6.5 shows the effective length as a function of the absorption coefficient change, Δα (= α_{off} - α_{on}), with different *r* under the maxima-power-difference condition. Since the QCSE is a very strong absorption effect, it only requires a short device length. Under moderate conditions (such as Δα > 3000cm^{-1} or *r* = 3), the optimal effective length is less than 10 μm. For photonic devices integrated with CMOS chips, it is actually critical to have small device sizes when other MOS devices have been scaled into the sub-100nm region.

6.3 Comparisons of Modulator Configurations

Modulator type	Vertical (AFPM)	Lateral (waveguide)
Cavity confinement	DBR mirror or reflection interface	Refractive index mismatch between Si, Ge, air, or oxide, nitride
Device size	Thicker layer with smaller surface area	Thin *i*-region and small width
Optical bandwidth	Low	High
Operation voltage	Several to tens Volt	<1V if only several QWs are used
Speed	High (reverse p-i-n diode, mainly RC limited)	
Optical coupling	Easy coupling	Taper structure required
Large scale integration	Free-space or fiber optics	2-D silicon waveguide available for large-scale planar integration

Table 6.1: Comparison between vertical and lateral modulators.

Table 6.1 compares several modulator merits of the vertical and lateral configurations. The build-up of waveguide confinement is relatively easier for lateral modulators since it can utilize the refractive index difference between Si and Ge as well as several typical CMOS-compatible dielectric materials, such as oxide, nitride, or even air. However, it is difficult for the SiGe system to produce the same vertical reflector technology as the III-V compound systems. Besides, the area of lateral modulators can be smaller than that of vertical devices because the lateral width of waveguides can be smaller than 0.5 μm while the diameter of AFPMs is larger than 6 μm. Lateral modulators need only several QW pairs, benefiting the precise growth control and low operation voltage. When only one or several output ports are necessary, the vertical configuration is preferred due to the ease of optical coupling; however, the mature Si-based waveguide technology makes the lateral integration a better candidate to achieve large-scale OEIC.

6.4 Optical Interconnections

Fig. 6.6 shows an optical system based on lateral modulators with waveguide channels. Since the QCSE is an electroabsorption effect, Ge/SiGe quantum well devices are not only optical modulators but also inherently photodetectors (for both lateral [108] and vertical [109] configurations). The process steps for modulators also build photodetectors at the same time, and then another Si-rich SiGe deposition step provides slabs without background absorption for the waveguide channels. It is also possible to build a similar structure based on a SOI wafer and use the top silicon layer as the light waveguide layer. Light supplied by an off-chip laser can be coupled into the modulator, carry the modulation signal (transmitter), pass through the waveguide in the same chip or be fiber-coupled into other chips (channel), and finally be absorbed by the detector (receiver). This approach is promising for all-group-IV optical interconnections.

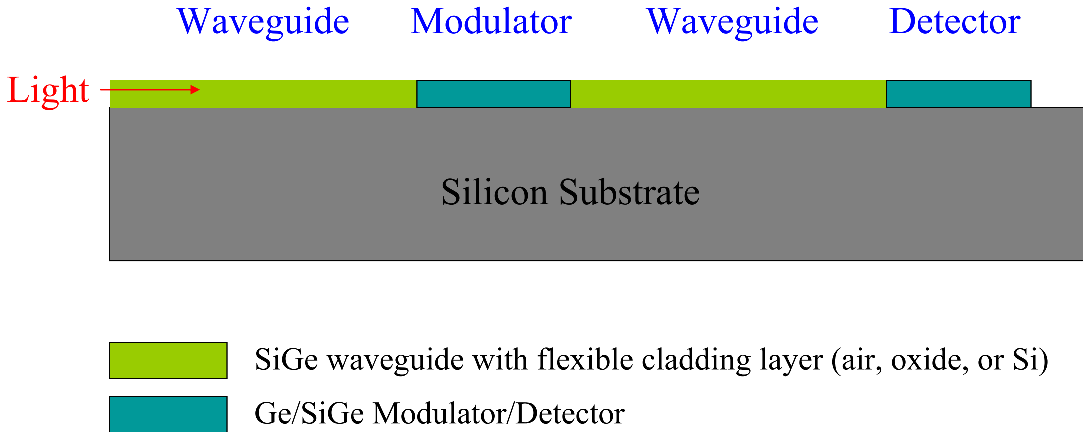

Figure 6.6: Optical interconnects based on Ge/SiGe modulator and detector as well as SiGe/Si waveguide. A similar structure with waveguides based on SOI is also possible.

Chapter 7 Conclusions

7.1 Summary

This dissertation described an investigation of germanium-silicon electroabsorption modulators. The challenges of speed, power, and cost for future interconnections make it inevitable that optical interconnections will be used. In order to combine the advantages of silicon electronics and optical components, silicon-based photonics provide the best integration scheme. However, the key issue for silicon-based photonics has been the lack of an efficient optical modulation mechanism in silicon for transmitter-end applications. Several approaches have been reported by numerous groups, but electroabsorption-based modulators, which would be the strongest mechanism and best solution, had not been successfully realized. This led us to study the energy band engineering possibilities to realize SiGe-based electroabsorption modulators.

The quantum-confined Stark effect is the most efficient electroabsorption effect and the strongest modulation mechanism. However, it was only previously observed in direct band gap III-V compound semiconductors. Several SiGe-based approaches were tried, but the band alignment and indirect band transition did not provide an efficient modulation effect. Though both Si and Ge are indirect band gap materials, the unique

band structure of germanium at the zone center gives it strong absorption characteristics – a sharp absorption edge with high absorption coefficient. This work utilized this property and the direct band gap difference between Si and Ge to engineer type-I aligned Ge quantum well structures.

The challenges in the SiGe material system are the high lattice mismatch and lack of information for Ge-rich SiGe alloys. This work also investigated the material growth of SiGe in both a research-oriented MBE system and a production-oriented RPCVD system. The growth issues related to the lattice relaxation and surface morphology were studied. The structure of strain-balanced Ge/SiGe quantum wells on relaxed Ge-rich SiGe buffers was proposed to prevent the lattice relaxation and to have better control of strain in the quantum well region. The growth of device materials was done by RPCVD and material characterization by XRD and TEM showed high quantum well quality.

SiGe p-i-n devices grown on relaxed SiGe buffers on Si substrates with strained Ge/SiGe MQWs in the i-region were fabricated using CMOS-compatible processes with a low thermal budget. The experimental results demonstrated strong quantum-confined Stark effect. With proper quantum well design and operation in the high-temperature CMOS chip environment, the modulators cover the entire C-band wavelength region. The clarity of exciton peaks, the absorption coefficient change, and the absorption edge shift in Ge quantum well structures on Si are comparable to those of direct band gap III-V compounds at similar wavelengths. The experimental results also agree well with the tunneling resonance simulations.

Vertical and lateral modulator configurations were analyzed and compared. Vertical modulators have high contrast ratio but narrower optical bandwidth. Lateral devices have shorter device lengths compared to previous electro-optic schemes, and waveguide modulators are promising for large-scale optical circuits with the existing mature Si-based waveguide technology. This research work will enable efficient

germanium-silicon modulators for optical interconnections integrated with silicon chips.

7.2 Future Work

The study of Ge-Si modulators actually gives us not only more opportunities for integration of silicon-based photonics but also far more exciting options and questions to answer. Since the effect is academically interesting and also practical for commercial applications, more future works in both physical understanding and engineering aspects are necessary.

7.2.1 Waveguide Modulators

The next step is to fabricate lateral modulators because this will lead to all-group-IV optical interconnections on silicon. These can be wave-guided by SiGe on silicon substrates or silicon on SOI substrates. The fabrication of waveguides and the optical coupling between fibers, waveguides and modulators needs further investigation.

7.2.2 Basic Parameters and Physics

Traditional SiGe research focused on indirect band gap engineering near the Si-rich end for high-speed or radio-frequency electronic applications, with much less work directed at the direct band gap parameters of pure Ge for optical applications. The direct band gap structure and effective masses of SiGe alloys are relatively experimentally unknown and need investigations, though our simulations show their uncertainties might not have major impacts on the Ge electroabsorption effect. The refractive index characterization of SiGe at wavelengths ranging from 1.2 to 1.6 μm is also necessary for both resonant cavity and waveguide designs.

These devices are designed for optical interconnects with silicon electronics where the modulation speed limit is RC delay in reverse-biased p-i-n diodes, and hence practically, the system speed would be determined by extrinsic parasitics and slower silicon electronics. However, it is still interesting to see if the dual confinement in the conduction band gives carriers a shorter tunneling time which enhances the intrinsic device speed and prevents saturation effects.

7.2.3 Process Integration with CMOS Electronics

To integrate modulator devices with silicon electronics, several additional steps must be inserted into the standard CMOS process. The fabrication of modulators can be divided into three main stages: (i) SiGe buffer layer growth and annealing, (ii) Ge/SiGe quantum well growth, (iii) lithography, etching, and metallization steps. Stage (iiii) can be combined with back-end processes without adding extra masks and cost. Stage (ii) is done at 400 ºC and can be inserted between the poly-Si formation and local interconnection steps during MOS processes. The key issue is stage (i) - in order to prevent the buffer layers from being oxidized, it can be done either (1) before the gate oxidation but with a thick oxide protection layer to block oxygen diffusion during oxidation, or (2) between the oxidation and poly-Si deposition, or (3) after the poly-Si deposition. Further experiments are necessary to evaluate each of these suggestions.

Though the buffer layer growth/annealing works fine for research purposes, the over-half-hour annealing time is too long for mass production. Two ways to reduce the annealing time: (i) wafers are annealed in a batch so the average annealing time is broken down to less than 1 min/wafer; (ii) wafers are annealed at or above the melting temperature of the buffer. The first solution should work well; the 2nd solution might cause surface roughening but an extra CMP step would flatten the surface and the

threading dislocation density might be even lower than that of the graded buffer method and should clearly be investigated.

7.2.4 Light Emission

Though the use of off-chip lasers as the light sources is preferred for optical interconnections as discussed in Chapter 1, it is still tantalizing to realize efficient light emission in group-IV semiconductors on silicon. Numerous approaches for silicon-based LEDs or lasers have been proposed, but their efficiency is far less than that of III-V materials. A direct band gap group-IV material grown on Si would be the best solution. Though Si, Ge, and C are indirect band gap semiconductors, their alloys with another group-IV semimetal element, Sn, in specific compositions could transform them into a direct band gap material. Among them, Ge-rich GeSn is the most promising based on theoretical calculations [110] and absorption experiments [111]. However, the synthesis of GeSn requires special epitaxial techniques [112, 113] because it is immiscible in most compositions and its crystalline form is thermodynamically unstable. Also the lattice mismatch between GeSn and Si is even higher. Low-temperature MBE growth of GeSn quantum dots on silicon might solve these problems. If "direct band gap" GeSn "dots" can be realized "without defects", it will immediately produce a current injected group-IV laser on Si.

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